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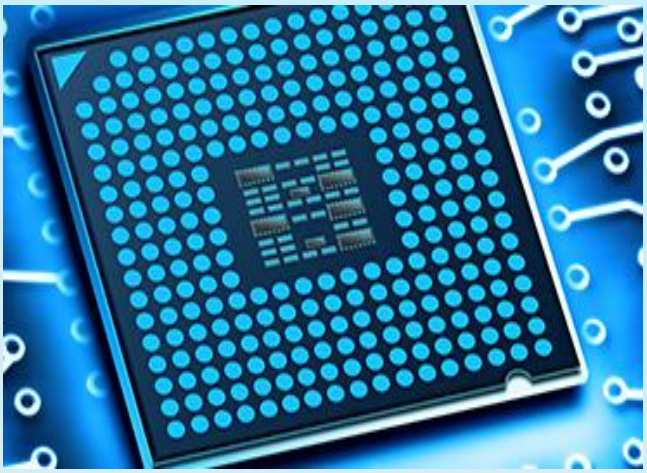
VLSI

MEMS



Transistor

PLL

Editor-in-Chief: Anirban Sengupta

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From the Editor-in-Chief's Desk - Editorial

The **IEEE VLSI Circuits and Systems Letter (VCAL)** is affiliated with the **Technical Committee on VLSI (TCVLSI) under the IEEE Computer Societ**y. It aims to report recent advances in VLSI technology, education and opportunities and, consequently, grow the research and education activities in the area. The letter, **published quarterly** (from 2018), covers the design methodologies for advanced VLSI circuit and systems, including digital circuits and systems, hardware security, design for protection, analog and radio-frequency circuits, as well as mixed-signal circuits and systems. The emphasis of TCVLSI falls on integrating the design, secured computer-aided design, fabrication, application, and business aspects of VLSI while encompassing both hardware and software.

IEEE TCVLSI sponsors a number of premium conferences and workshops, including, but not limited to, ASAP, ASYNC,ISVLSI, IWLS, SLIP, and ARITH. Emerging research topics and state-of-the-art advances on VLSI circuits and systems are reported at these events on a regular basis. Best paper awards are selected at these conferences to promote the high quality research work each year. In addition to these research activities, TCVLSI also supports a variety of educational activities related to TCVLSI. Several student travel grants are sponsored by TCVLSI in the following meetings: ASAP2018, ISVLSI 2018, IWLS 2018, iSES 2018(formerly iNIS 2017) and SLIP 2018. Funds are provided to compensate student travels to these meetings as well as attract more student participation. The organizing committees of these meetings undertake the task of selecting right candidates for these awards.

The current issue of VCAL showcases the state-of-the-art developments covering several important areas: MEMS Based Low Power Efficient Capacitive Inverter, Degenerate Pass-Transistor Logic, digital second order generalized integrator (SOGI) phase locked loop (PLL). The peer-reviewed articles can be found in the section of "Features Articles". In the section of "Updates", upcoming conferences/workshops, call for papers and proposals, funding opportunities, job openings, conference report and Ph.D. fellowships are summarized. Additionally, a "Member News" section has been started from past issue onward covering the achievements of TCVLSI members.

I would like to express my appreciation to the outgoing Co-EiC of VCAL, Saraju P. Mohanty for his exemplary services during his editorial term: 2015 – 2019. I would also like to thank all editorial board members (Yiyu Shi, Himanshu Thapliyal, Michael Hübner, Nicolas Sklavos, Jun Tao Shiyan Hu, Hideharu Amano, Mike Borowczak, Helen Li, Saket Srivastava, Yasuhiro Takahashi, Sergio Saponara, James Stine and Qi Zhu) for their dedicated effort and strong support in organizing this letter. The complete editorial board information is available at: https://www.computer.org/web/tcvlsi/editorial-board. We are thankful to our web chair Mike Borowczak, for his professional service to make the letter publicly available. We wish to thank all authors who have contributed their professional articles to this issue. We hope that you will have an enjoyable moment when reading the letter! The call for contributions for the next issue is available at the end of this issue and we encourage you to submit articles, news, etc. to an associate editor covering that scope.

Anirban Sengupta
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Features

MEMS Based Low Power Efficient Capacitive Inverter for renewable energy applications

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Abstract – In this paper, a micron sized DC/AC power inverter design based on MEMS (micro electromechanical system) is proposed, modeled and demonstrated. The proposed approach uses electrostatic actuation to provide in phase overlap length varying DC/AC inverter system for solar cell application. Two MEMS structures are considered to show good electrical and mechanical performance with zero harmonics and negligible power loss. Also, the actuation voltage is provided under pull in voltage to the actuating part, so that maximum displacement of overlap length is acquired with less instability. The proposed micro scale system exhibits miniaturized volume and expected to acquire improved performance of DC/AC power inverter used for renewable energy applications.

1. Introduction

Power inverters are one of the major concerns to be taken care of, in most of the alternative energy systems for the conversion of DC which is obtained from photovoltaic generators into AC. Several researches are going on these days to improve the efficiency of these high rated power inverters [1]. In semiconductor industries, conventional high rated power inverters based on Si power semiconductor device (PSD)are facilitated [2-3].But, it has several demerits like On-state loss, switching loss of power devices, complex control system configurations, low efficiency, high costs and all these demerits are partially eliminated by PWM Multilevel inverters [4-5].Even then major challenges are present towards large number of switches to be controlled in multilevel power inverter that causes complexity, presence of harmonics that causes high leakage current and also many more deficiencies strongly affect the DC/AC conversion quality performance. On the other hand, MEMS Inverter approach was proposed as an alternative [6-7]. The micromachining technology that had emerged in the late 1980s [8] is one of the most attracting field in the electronics and electrical engineering domain. There are wider application fields of MEMS technology like as, RF-MEMS [9-13], biomedical [14], Aerodynamics [15], thermodynamics [16], telecommunication [17] and so on. It is the well-established technology that provides the low power-actuation, low- cost production and miniaturized volume devices [18-20]. To design the MEMS inverter with the low power-actuation, low- cost production and miniaturized volume, researchers faced several challenges.

In this paper, the goal is to demonstrate an implementation of proposed design and mathematical modelling of electromechanical DC/AC inverter system of micron size. The proposed MEMS design is based on comb drive structure for the formation of two sets of variable capacitor (driver and converter). One with two sets of electrodes where one is moving (makes the capacitor variable by to and fro movement) and other is fixed. Moreover, the electrostatic actuation is accomplished by external electrical AC signal to the driving capacitor, thereby enabling variation of overlap length of the converter capacitor for the conversion of solar DC input to AC output. The proposed design is simulated in COMSOL 5.0 to see the resulting mechanical movement of electrodes. On the basis of the design, mathematical expressions are modelled using MATLAB 2013for suitable desired electrical performance.

2. Physical modelling of system design

The design consists of fixed comb electrodes (fixed on anchors), moving comb electrodes, a proof mass (substrate) suspended by double folded flexure (having beams, trusses and anchors) beams and a shuttle mass through which moving comb finger electrodes set attached to the substrate (moving mass) as shown in Figure 1. In this design two capacitive sets formed, exhibit in-phase deflection of overlap lengths when subjected to mechanical movement of moving electrodes

which actually means when the capacitance of one set is increased, the other set of capacitance is also increased. And this deflection makes the capacitors variable in nature where one set of capacitors is working as driving part and other set as converter part of the system.

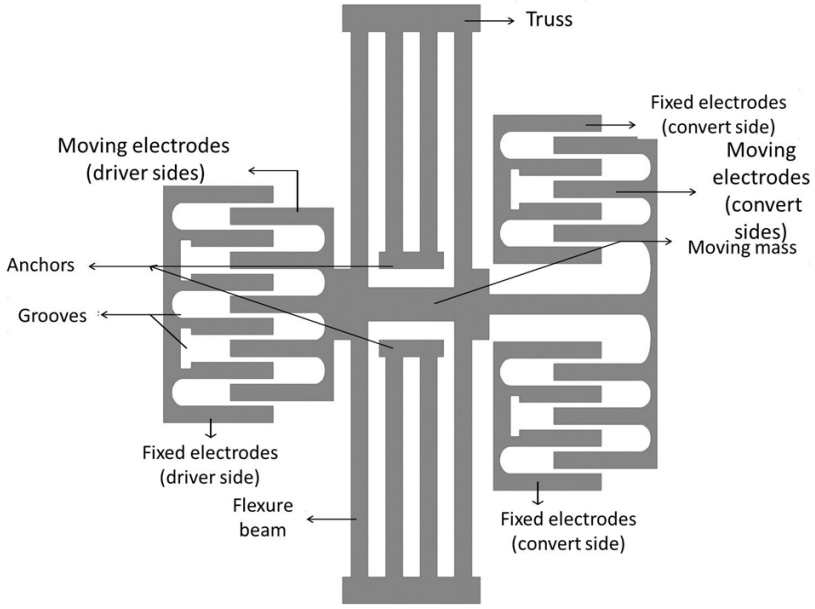

Figure 1: Schematic View of System Design of MEMS Power Inverter.

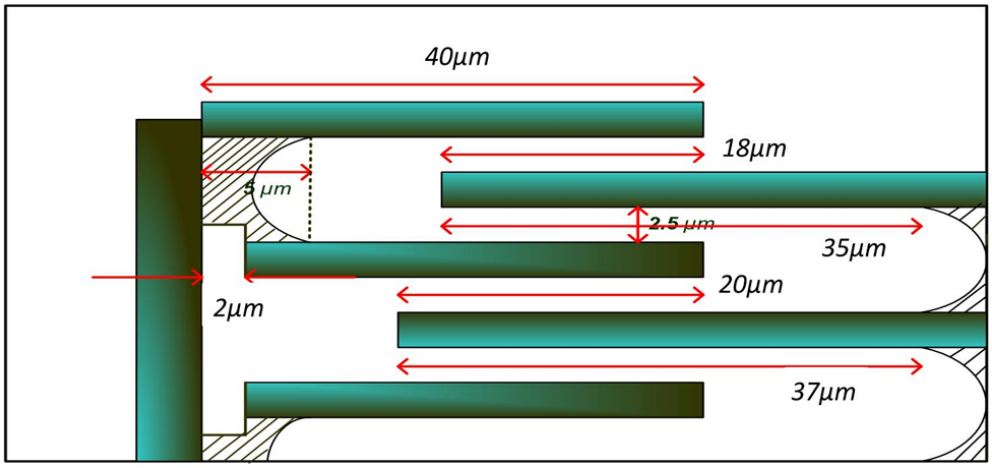

Figure 2: A small part of proposed Interdigitated Capacitor Design (ICD).

The sketch of a small part of the design of comb structure proposed is shown in Figure 2. In the capacitive portion, one moving finger is kept smaller and the next finger of it is kept 1 to 2 µm larger than the previous finger expecting to reduce the fringing effect and to acquire more capacitance formation than the previous work [21].Also, the proposed design consists of groove shaped structure expecting to reduce the front instability of front part of electrodes as because when the actuation is done, not a single pair of capacitor is formed but more than one capacitance is formed [22]. To lessen the effect of the other pair of capacitors, all these changes in capacitor geometry have been done. Thus sample of the proposed design is implemented by using optimization method (using COMSOL 5.0) in which the comb structure (consisting of moving and fixed limbs) is attached to the double folded flexure [23] spring through the moving mass. The detailed specification of the design and the basic materials used are depicted based on the references [24, 25].

3. Operating principle and mathematical representation of MEMS comb structure

The specifications of inputs are provided in Table 1. The equivalent electrical circuit diagram of the proposed system is shown in the Figure 3.

Table 1 Specifications of the input provided to the system designed

INPUT	VALUES
Reference DC Voltage	23.3 V
Reference AC Perturbed voltage	220 V
Frequency	50- 60 Hz (Range)
Solar DC input	24 V
Load(resistive)	10 KΩ

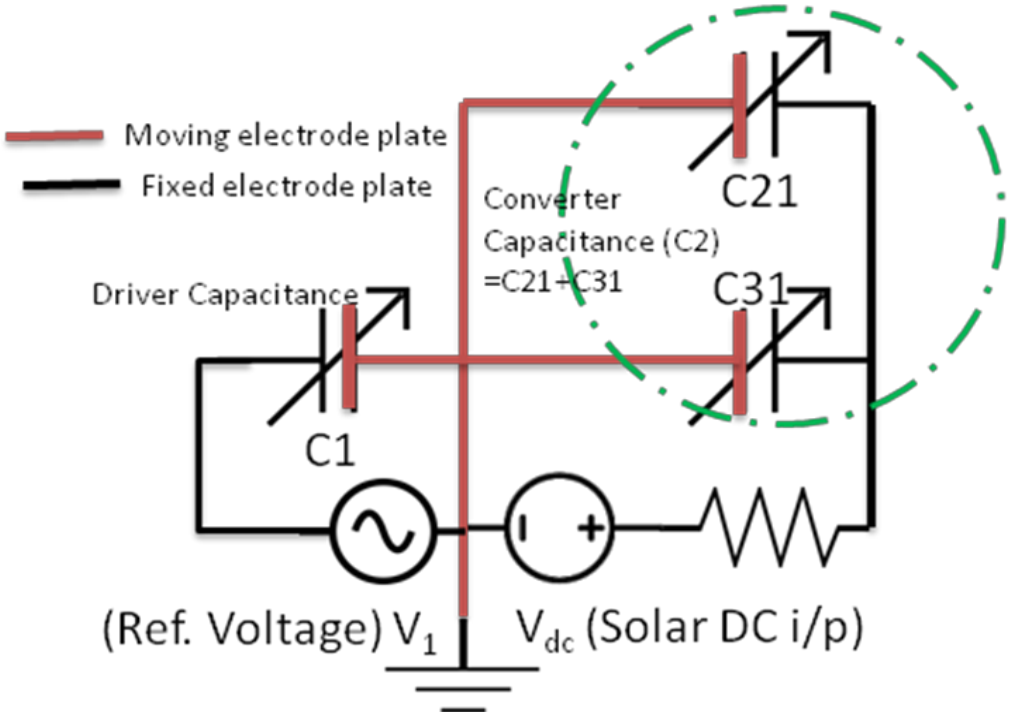

Figure 3: Equivalent Circuit Diagram of MEMS Power Inverter.

Actuating voltage applied on the driving comb structures results in a deflection of the moving fingers in both X and Y directions, but it is preferably in desired Y direction with a small deflection in undesired X-direction because of presence of double folded flexure [21]. The capacitance depends on the geometry of capacitor, not on the applied actuation voltage or accumulated charge. Hence this deflection causes change in overlapping length (l_0) and thus the area changes which finally results in variation of capacitance ($C_{var}(t)$) expressed as equation (1).

$$C = \frac{\varepsilon_0 \varepsilon_r N_e \left(L_0 + \bar{X}\right) t_e}{g} \qquad (1)$$

where ε_0 = Permittivity of vacuum (8.854×10^{-12} F/m), ε_r =Medium dielectric constant (1 for vacuum), N_e = Number of movable capacitor's electrodes, L_0 = Electrode's initial overlapping length, t_e = Electrode's thickness, g = The gap between movable and fixed electrodes. An equal and opposite charges build on the surface of electrodes due to the potential difference between the electrodes (fixed and moving) because of which electrostatic force (F_{es}) developed in between the electrodes is

$$F_{es} = \frac{1}{2}\left(\frac{dC_{\text{var}}(t)}{dy}\right)V^2 = \frac{1}{2}\left[\left(\frac{dC_1(t)}{dy}\right)V_1^2 + \left(\frac{dC_2(t)}{dy}\right)V_{2\,\text{var}}(t)^2\right] \qquad (2)$$

Where, $C_1(t)$ =Driving capacitance, $C_2(t)$ =Equivalent converter capacitance in which the two sets of capacitor are connected in parallel shown in the Figure 4 is

$$C_2(t) = C_{2i} + C_{3j} \quad \text{where} \quad i, j = 1,2,3....N_e \tag{3}$$

$$\frac{dC_{\text{var}}(t)}{dy} = \begin{Bmatrix} \frac{C_0}{I_0}, \bar{y} = y \\ \frac{-C_0}{I_0}, \bar{y} = y \end{Bmatrix}$$, Rate of change of capacitance with displacement

Where V_1 = Driving voltage or reference voltage

$$V_1 = \sqrt{(V_{AC}{}^2) + +(V_{1DC}{}^2)} \tag{4}$$

Where, V_{1DC} = Reference DC bias Voltage, V_{AC} = AC perturbed reference voltage. V_1 can be varied so as to change the amount of charge (Q_{c1}) accumulated on the surface of electrodes and moving electrodes allow the use of that charge ($Q_{c2}(t)$) as an intermediate variable which can be used to control the change in l_0 so that $C_2(t)$ is increased and voltage ($V_{2\text{var}}(t)$) across $C_2(t)$

$$V_{2\text{var}}(t) = \frac{1}{c_2(t)} \int i_{\text{var}}(t) \partial t \tag{5}$$

By applying KVL in the electrical domain of converter side, the resulting relation is –

$$V_{2\text{var}}(t) = V_{DC} - R_L i_{\text{var}}(t) \tag{6}$$

Where V_{DC} = Solar DC input voltage , R_L = Load Resistance, $i_{Var}(t)$ = Current in the converter circuit

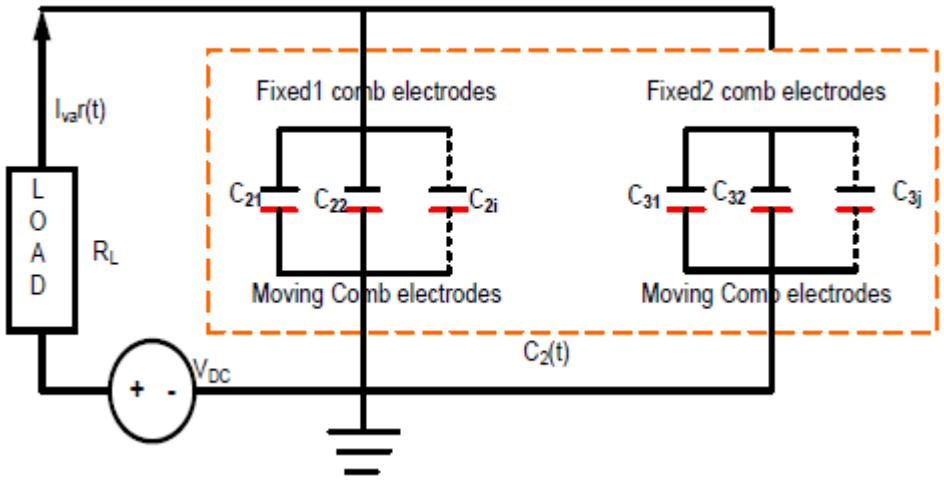

Figure 4: Converter Circuit Diagram in Electrical Domain.

$$i_{\text{var}}(t) = \frac{dQ_{c2}(t)}{dt} = \frac{d}{dt}[C_2(t) V_{2\text{var}}(t)] \tag{7}$$

$$i_{\text{var}}(t) = V_{2\text{var}}(t)\left[\frac{dC_2(t)}{dt}\right] + C_2(t)\left[\frac{dv_{2\text{var}}(t)}{dt}\right] \tag{8}$$

$$V_{DC} - \left\{ \frac{C_2(t) R_L \left[\frac{di_{\text{var}}(t)}{dt} \right]}{\frac{dC_2(t)}{dt}} \right\} - \left\{ R_L + \frac{1}{\frac{dC_2(t)}{dt}} \right\} i_{\text{var}}(t) = 0 \tag{9}$$

$$V_{DC} - L_2(t) \left[\frac{di_{\text{var}}(t)}{dt} \right] - \{R_L + R_2(t)\} i_{\text{var}}(t) = 0 \tag{10}$$

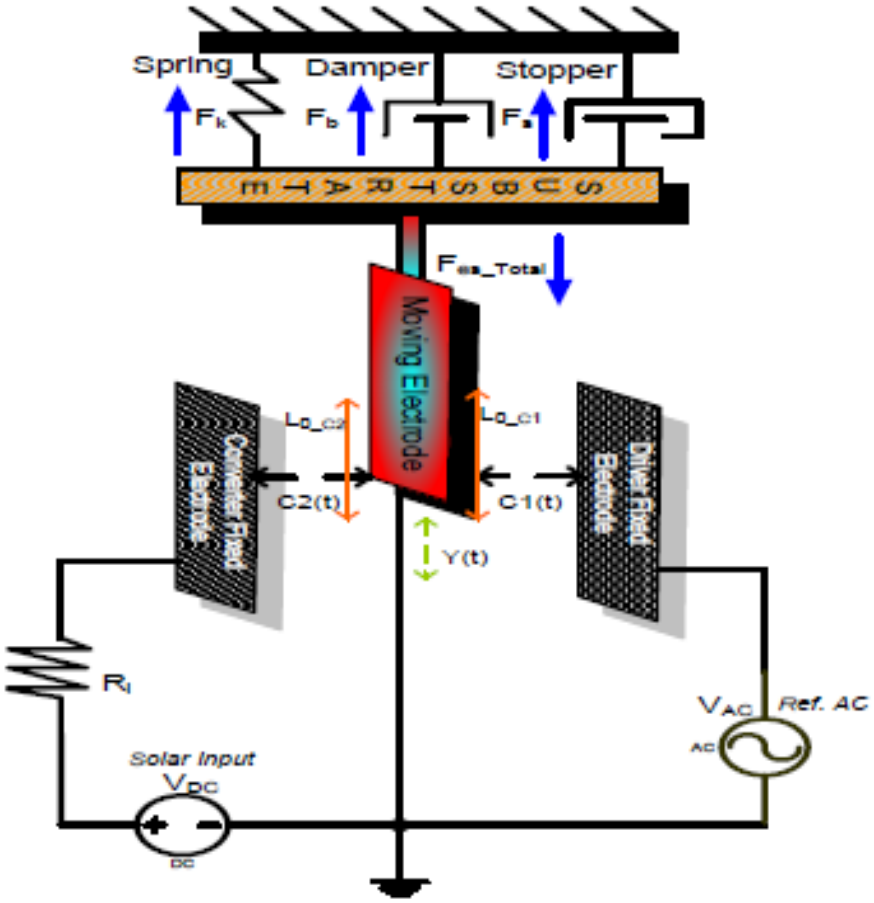

Figure 5: Simplified Circuit Diagram of the proposed MEMS inverter.

The equation (**7**) represents the converter circuit consists of source V_{DC} in series with [varying inductor $L_2(t)$) and varying resistor ($R_2(t)$) as new components [18] of] $C_2(t)$ and R_L

$$R_2(t) = \left[\frac{1}{\frac{dC_2(t)}{dt}} \right] \tag{11}$$

$$L_2(t) = \left[\frac{R_L C_2(t)}{\frac{dC_2(t)}{dt}} \right] \quad (12)$$

Where, inductive part (9) represents the energy storage element results from coupling between the capacitor converter circuit and the load resistance. Resistive part (8) represents the open circuit resistance meant for the measure of energy dissipation i.e. for minimum internal resistance; we require increment in the value of rate of change of capacitance. Continuously growing of electrostatic force causes the displacement in positive Y-direction. In order to keep the electrodes away from 'esp of bursting', an equal and opposite force resisting this motion is modeled by restoring force [26-28] of a mechanical spring with spring constant (k) and a damper with damping coefficient (b_m). The total force acting on the system design is shown in the Figure 5.

The balance force is defined as equation 10.

$$my + b_m y + ky + F_s = mA_{es} + F_{es} \quad (13)$$

The term, mechanical stopper force (F_s) is the resultant mechanical force used to limit the deflection of moving mass by

$$F_s = \begin{Bmatrix} 0, & -y_s \le y \le y_s \\ k_s(y + y_s), & y < -y_s \\ k_s(y - y_s), & y > y_s \end{Bmatrix}$$

Where, k_s =Stiffness constant of stopper $\pm y_s$ = Moving mass deflection limit.

4. Results and discussion

Mathematical modeling of the proposed MEMS power inverter is simulated using MATLAB Simulink to determine the resulting plots of converted AC voltage and force versus displacement shown in the Fig 6. It is observed from the plots that converted AC voltage obtained is of amplitude 4.7V across the Load (10 KΩ) at the solar input of 19.6V when the system is being actuated by reference of 130V, 50 Hz; AC and 3V; DC bias voltage for 2 seconds. The electrostatic force built up to 16.6× 10^-4 N which facilitates the maximum displacement of overlap length up to 9 μm.

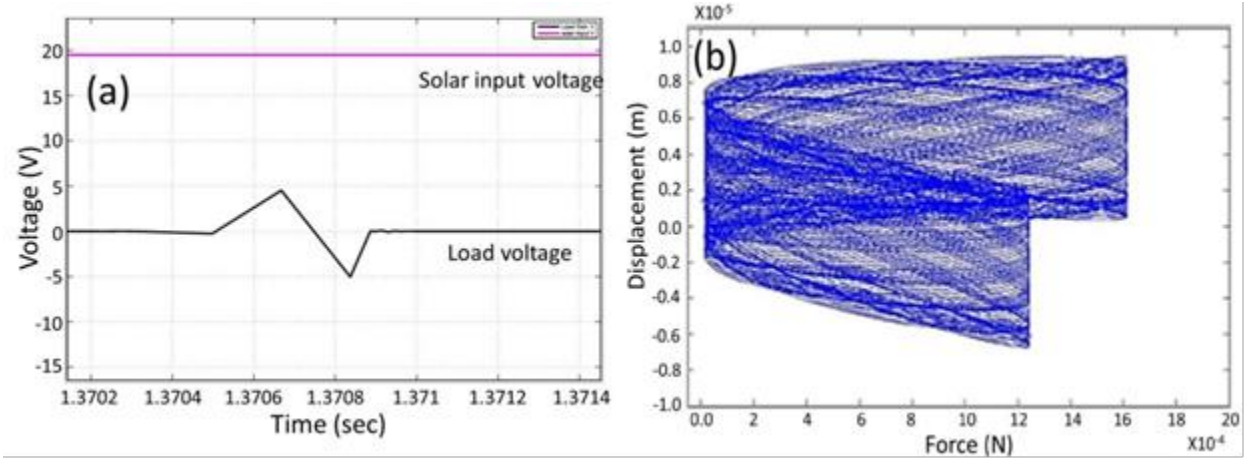

Figure 6: Converted Voltage across Load with Solar Input Voltage Versus time Plot, (b) Force Built up Versus Displacement Plot

For the concept demonstration and the comparison purposes, only a half part of the proposed design is simulated in COMSOL 5.0 Multiphysics taking two cases (a) simple rectangular and (b) modified rectangular grooved comb drive structure. Comparisons of two different cases (models) are done on the basis of the following parameters like electric potential distribution, displacement and capacitance variation. The resulting surface plot of electric potential distribution and the displacement facilitated by actuation voltage of 23.3V for both the models. Also, the displacement and capacitance variation with respect to the applied voltage can be seen and measured clearly from Fig.7.

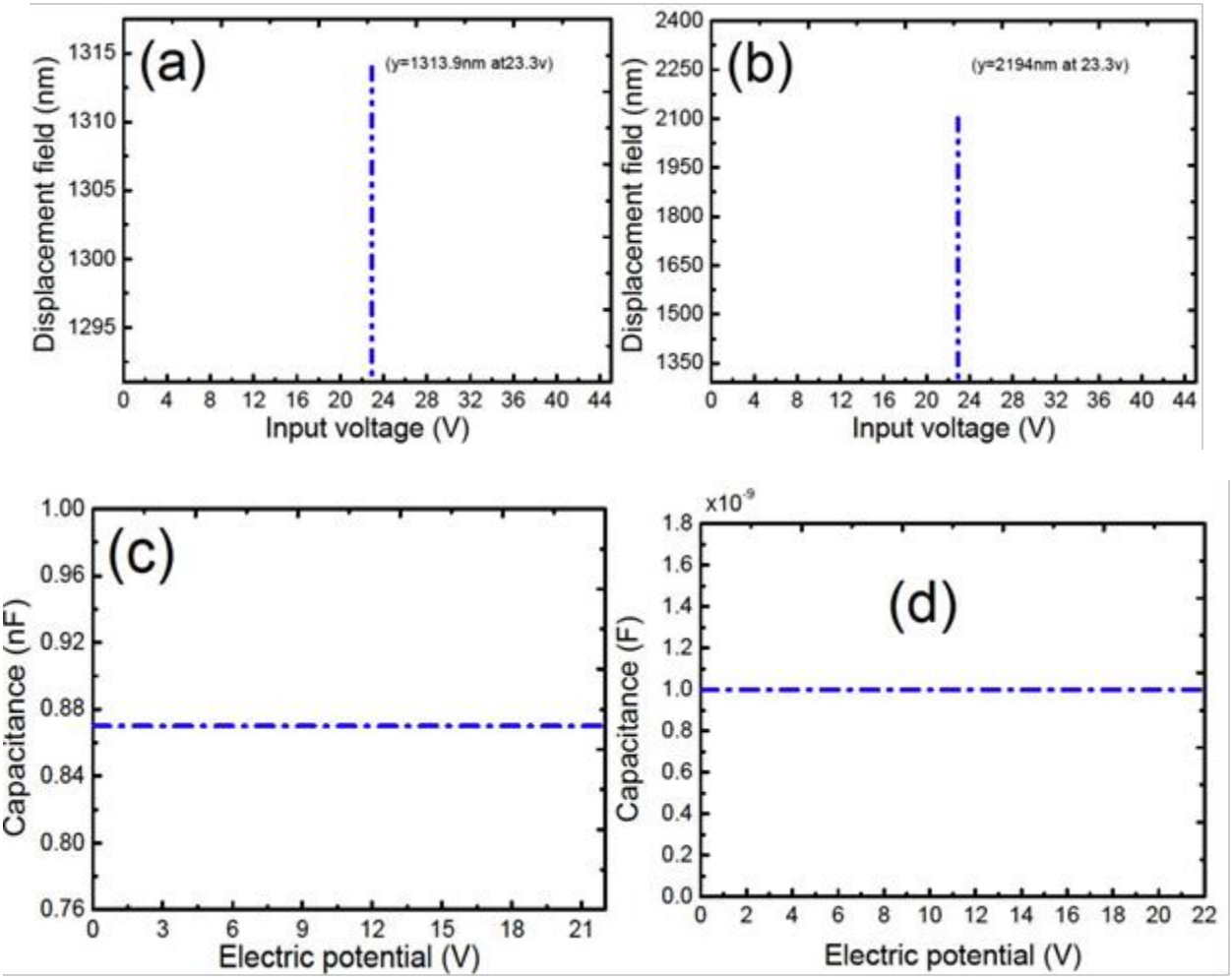

Figure 7: (a), (b) Displacement(y) Vs applied Voltage for both the models (1 & 2), (c)(d) Capacitance(C) Vs. Electric Potential for both the models (1 & 2) (C=0.8701nFC=0.9623 n)

Table 2 Resulting Values of Plot 7

DESCRIPTION	INPUT	MAXIMUM	CAPACITANCE
	VOLTAGE	DISPLACEMENT	VALUE
Model 1	23.3 V	(1289.7-1313.9) nm	0.8701 nF
Model 2	23.3 V	(2189.6-2194) nm	0.9623 nF

It is seen in figure 7 that the displacement and capacitance values of case I are more than case 2 (table 2). Actuation depends on the number of comb fingers [24] which is related to electrostatic force and capacitance. Surface electric potential and displacement plot of the moving electrodes are observed so that the capacitance formed due to the fixed and moving electrodes are being varied and the graphs are obtained and shown in the figure 8. Displacement shown in the fig. 8 (b) is towards the Y-direction that actually meant for the enhancement of the overlap length of the capacitors because of which the overlapping area increases. The increase in overlapping area facilitates the increase of capacitance across the converter circuit.

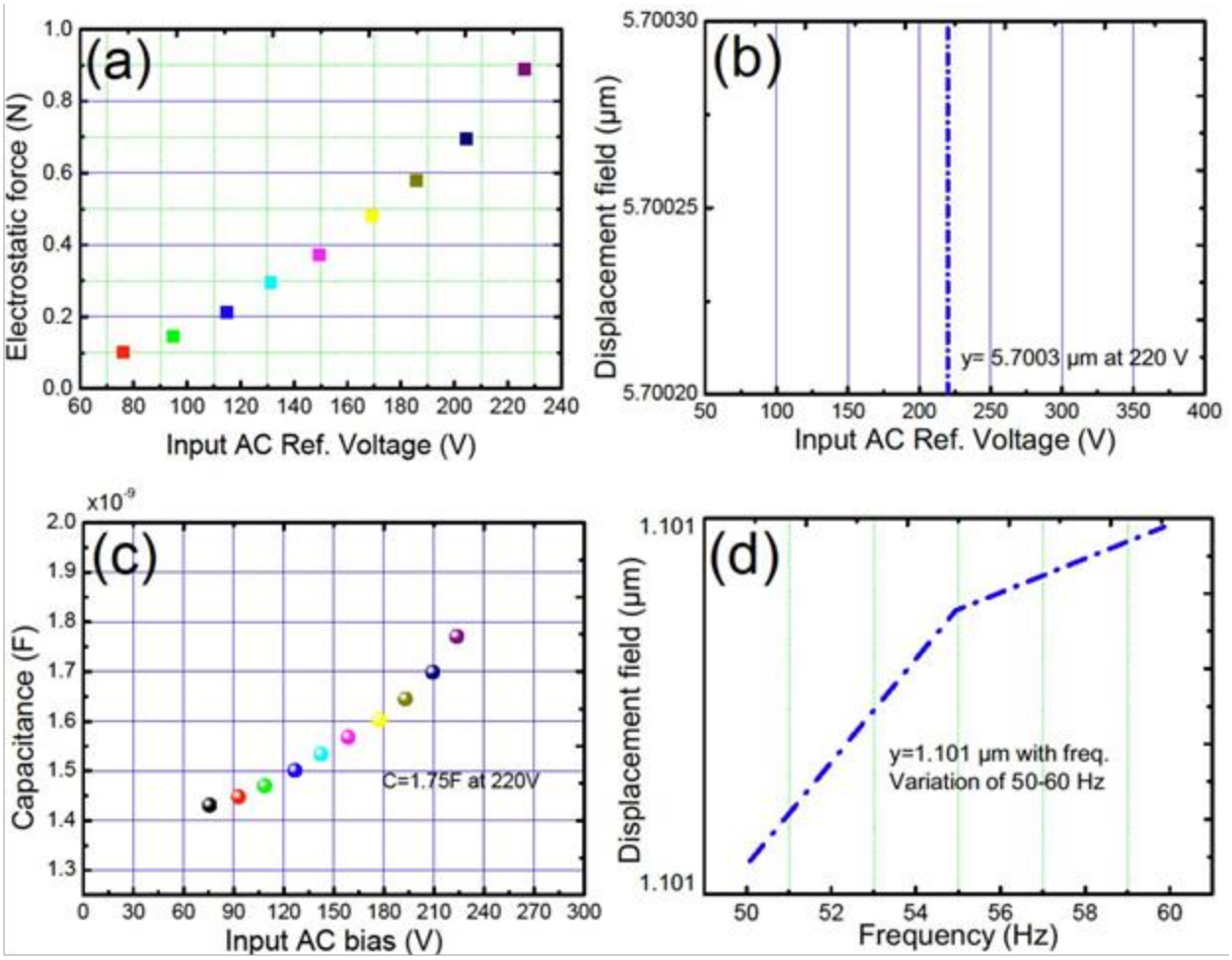

Figure 8: (a) Electrostatic force (F) Vs Reference Voltage (F= 0.84 N at 220 V), (b) Displacement (y) Vs Actuation Voltage (V), (c) Capacitance (C) Vs Actuation Voltage, (d) Displacement (y) versus Frequency (f) (Hz).

From the plots in Figure 8, it is seen that due to the actuation voltage, the electrostatic force is built up in between the two electrodes (fixed and moving) which is proportional to the square of the applied voltage and its variation with different values of voltage is shown by the plot 8(a). The electrostatic force further causes the displacement in overlap length which then induces change in capacitance and as the capacitance is inversely proportional to the voltage; here its variation with voltage is shown in Fig. 8(c). Also, the displacement depends on the frequency of the AC perturbed reference voltage which can be clearly shown by the plot (d) of Figure 8. Low power VLSI application is major concert in the current technology [29, 30]. The proposed model is applicable for low cost and low power application.

5. Conclusion

This paper proposed a solution to the critical problem of DC/AC conversion quality performance of commercial power inverter used for renewable energy applications by adopting the MEMS based capacitive power inverter system. Owing to the proposed concept, mechanical part of the system is designed to have a high level of stiffness in order to be actuated by the power grid voltage. The proposed MEMS approach enables the non-complexity of the inverter, zero harmonics, miniaturized volume device, low cost production and very less losses (almost lossless). It also doesn't consume power for the DC/AC conversion process. It is developed in this work by means of simulations of two models for comparison and the modified comb drive design is proposed so as to lessen the instabilities with acquisition of more capacitance formation across interdigitated electrodes so that it can be directly used in MEMS capacitive Transducer.

Acknowledgement: The respective work was supported by Jadavpur University so that the design is simulated in COMSOL 5.0 to see the resulting movement of mechanical part of the system after being actuated electrically.

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Features

An Energy-Efficient High-Performance 8-Transistors Full Adder Cell Based on Degenerate Pass-Transistor Logic

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Abstract – In this paper, a new design of 8 transistors full adder cell based on pass transistor logic has been proposed. The proposed full adder cell consists of three modules of which two are XOR module and one OR module. The proposed full adder cell has improvement in different performance parameters like leakage current, power dissipation, delay, and area. All the simulations are performed at 65 nm technology node using Synopsys HSPICE simulator. The proposed 8T full adder circuit has better control in leakage current, static power, and dynamic power dissipation. The dynamic power dissipation of proposed full adder cell 8T_DPTL is smallest as compared to all other cells. The proposed 8T_DPTL full adder cell is 58.7% faster and required 20% less chip area as compared to 6T full adder cell. The proposed full adder cell has the maximum degradation of 11% of the output level compared with 17.44% degradation for 6T full adder cell. The figure of merit of the proposed full adder cell is 189.4 times better as compared to 6T full adder cell means the proposed cell is best suited for the low power, high performance, and high computing applications.

1. Introduction

With the increased usage of the battery-operated portable devices like cellular phones, portable personal communication systems, and notebooks demand VLSI and ultra-large-scale integration designs with the improved power delay characteristics [1]. Many computing intensive applications such as multimedia processing, digital computing can now be realized to either speed up the operation and/or reduce the power/energy consumption. Full Adder (FA) is one of the most critical components of a processor, as it is used in the arithmetic logic unit, floating-point unit, and address generation for memory accesses [2][3]. The essence of digital computing lies in the full adder design. The design criteria of a full adder are usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as the multiplier and arithmetic logic unit (ALU). There are many full adder designs have been proposed targeting on various design emphases such as power, speed, and circuit complexity. Among them, low transistor counts full adder designs based on degenerate pass transistor logic (DPTL) have been actively pursued to reduce the circuit complexity for low power operations [4].

Various designs of low power full adder cells can be found in the different kinds of literature. The conventional CMOS full adder cell required 32 transistors and its modified version required 28 transistors [5]. As the transistor count is high the design complexity for ALU will increase drastically and hence it required the circuits which have fewer transistor counts to perform the same operation. Several low transistors count full adder circuits have been proposed in the literature such as 6T [6], 7T_UB (7T with upper buffer) [7], 7T_LDPTL (7T with lower DPTL) [8], 8T_BB (8T with both buffer) [9], 10T_PTL (10T with pass transistor logic) [10], and hybrid adder [11] etc. as shown in Figure 1(a)-(e). The main goal of these circuit design techniques is improved circuit performance, especially in low transistor count full adder circuits.

The paper is organized as follows: Section 2 describes the proposed 8 transistors full adder cell, Section 3 provides the simulation results and performance characteristics of different full adder cells. The concluding remarks are given in Section 4.

2. Proposed 8T Full Adder Cell

Proposed full adder cell consists of 8 transistors as shown in Figure 1(f). In the proposed circuit, a first level XOR logic is performed by using degenerate pass transistor logic which consists of 4 transistors. Further the output of XOR act as a control signal to generate both sum and carry logic. To generate sum, a 2 transistor XOR logic is used where two signals (C and $\bar{C}$) are passed according to the logic of level one XOR block whereas to generate carry, a 2-transistor pass logic is used where two different signals (A and C) are passed according to the logic of level one XOR block. The first

level XOR logic with 2 transistors of Figure 1(a) has been replaced by 4 transistor XOR logic to improve the output levels of both the sum and carry. The generalized equations of the sum and carry for the proposed circuit can be expressed as:

$$\text{Sum} = (\text{A} \oplus \text{B})\,\bar{\text{C}} + \overline{(\text{A} \oplus \text{B})}\text{C} = \text{A} \oplus \text{B} \oplus \text{C} \quad (1)$$

$$\text{Carry} = \overline{(\text{A} \oplus \text{B})}\text{A} + (\text{A} \oplus \text{B})\,\text{C} = \text{AB} + \text{BC} + \text{CA} \quad (2)$$

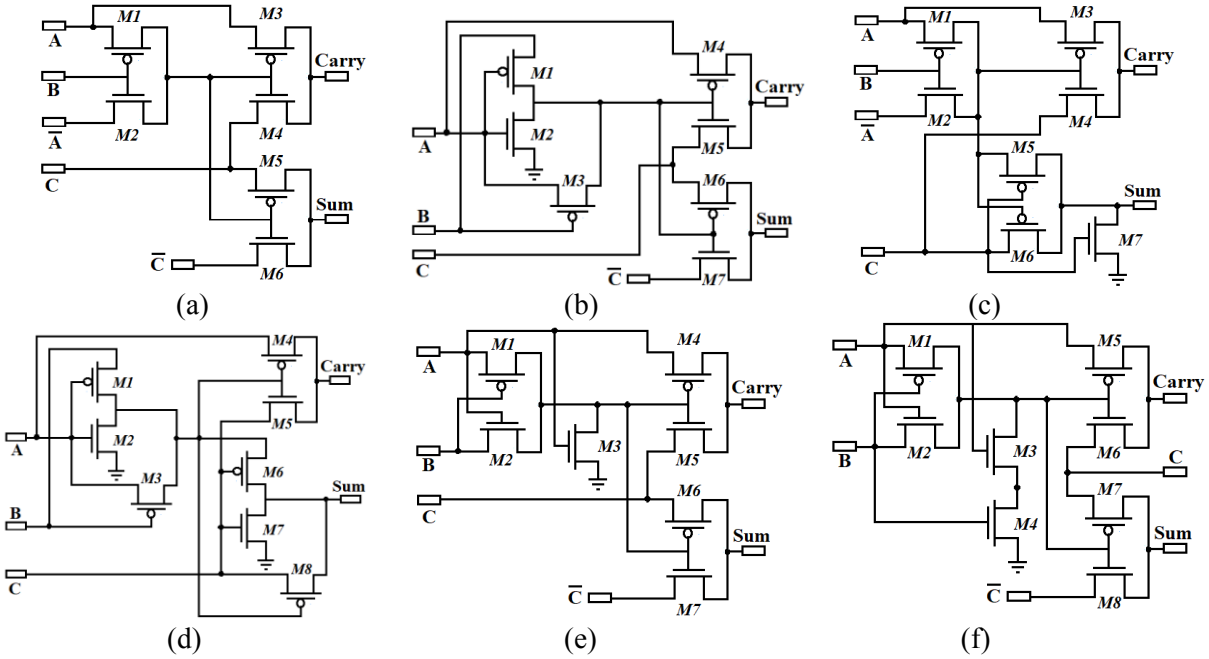

Figure 1: Different one-bit full adder cells: (a) 6T (b) 7T_UB (c) 7T_LDPTL (d) 8T_BB (e) 7T_DPTL (f) 8T_DPTL

A. Leakage Current Estimation of Proposed Full Adder Cell

The leakage current of the circuit is the major issue in deep submicron technology. The leakage current is the major promoter in the total power dissipation of the circuit especially for those circuits which are idle for most of the time. In any of the CMOS circuit, subthreshold leakage current (I_{sub}), junction leakage current (I_{jn}) and gate leakage current (I_g) are the major components of short channel effects in the devices.

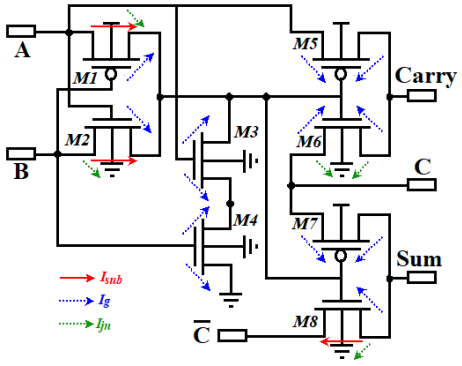

Figure 2: Leakage current estimation of proposed 8T_DPTL full adder cell.

The major leakage current components for proposed 8T_DPTL full adder cell for worst case input combination ABC = 111 as shown in Figure 2 and given by:

$$I_{sub,111} = I_{sub,M1} + I_{sub,M2} + I_{sub,M8} \quad (3)$$

$$I_{g,111} = I_{gd,M1} + I_{gs,M2} + I_{gd,M3} + I_{gs,M3} + I_{gd,M4} + I_{gs,M4} + I_{gd,M5} + I_{gs,M5} + I_{gd,M6} + I_{gs,M6} + I_{gd,M7} + I_{gs,M7} + I_{gs,M8} \quad (4)$$

$$I_{jn,111} = I_{jnd,M1} + I_{jnd,M2} + I_{jnd,M6} + I_{jns,M6} + I_{jns,M8} \quad (5)$$

$$\boldsymbol{I_{Leakage,111} = I_{sub,111} + I_{g,111} + I_{jn,111}} \quad (6)$$

From the above leakage current estimation, we can observe that the proposed full adder cell has a maximum component of I_g which shows that gate leakage current has maximum contribution to the total leakage current. The I_g component has more effect with the technology scale down.

TABLE 1
TRUTH TABLE OF PROPOSED 8T_DPTL FULL ADDER CELL @ V_{DD} = 0.9 V.

Input combinations			Logic outputs		Proposed FA output	
A	B	C	Sum	Carry	Sum	Carry
0	0	0	0	0	0.1	0
0	0	1	1	0	0.9	0
0	1	0	1	0	0.815	0
0	1	1	0	1	0	0.815
1	0	0	1	0	0.815	0
1	0	1	0	1	0	0.817
1	1	0	0	1	0.1	0.9
1	1	1	1	1	0.9	0.9

3. Simulation Results

In this section, the effectiveness of the proposed circuit is investigated using 65 nm technology node. The HSPICE simulator is used for the study of different full adder cells. 0.9V of supply voltage have been considered for the simulation at 27°C operating temperature. All the circuits are simulated at four different input frequencies 12.5 MHz, 25 MHz, 50 MHz, and 100 MHz to analyze the effect of input frequency on dynamic power dissipation. The output levels of the sum and carry for different input combinations for proposed 8T_DPTL full adder cell is given in Table 1. From the table, it is observed that the maximum degradation in the output swing is about 11% and 9.4% of both sum and carry for low logic and high logic, respectively. The simulated output waveform of proposed 8T_DPTL full adder cell is shown in Figure 3.

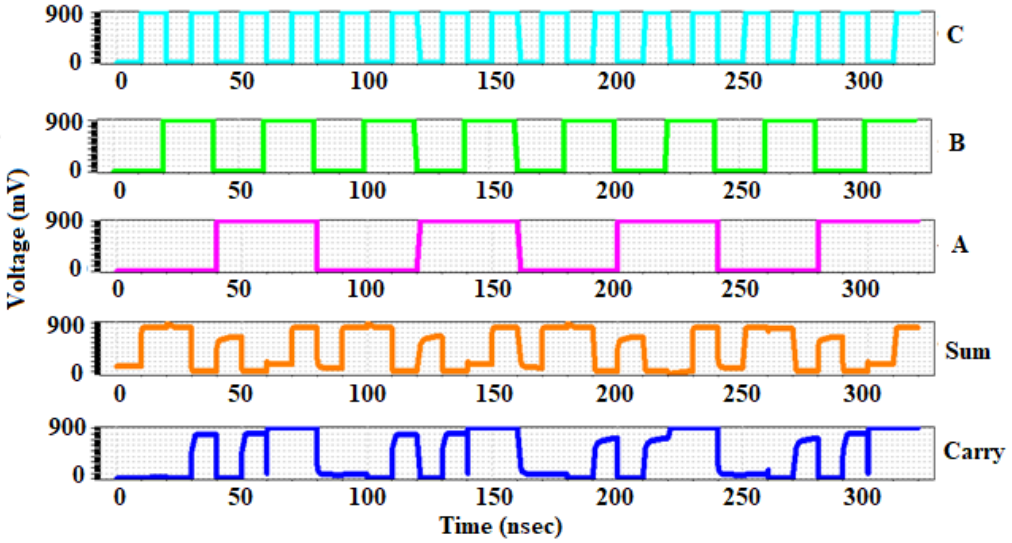

Figure 3: Output waveform of the proposed 8T_DPTL full adder circuit.

All the six full adders are based on pass transistor logic and have less transistor count. Because of pass transistor logic and less transistor count, the outputs (sum and carry) of full adder cell may be degraded within the acceptable margins. DC analysis results of different Full Adder designs are shown in Table 2. Cout_HI(min) and Sum_HI(min) are the minimum value of logic high of Carry and the logic high of Sum respectively whereas Cout_LO(max) and Sum_LO(max) are the maximum value of logic low of Carry and logic low of Sum respectively. From Table 2, it is observed that the maximum degradation in the logic levels for 8T_DPTL full adder cell is 0% and 9% for logic low and logic high for carry and 11% and 9% for logic low and logic high for sum respectively. The normalized values of all the parameters are given in Table 3.

A. Leakage Current Analysis

Figure 4 shows the leakage current for different full adder cells for all 8 input combinations. The proposed design circuits in most of the input combinations. Average leakage current is less for 7T_DPTL based full adder cell whereas the

proposed 8T_DPTL full adder cell also has sufficient leakage reduction as compared to 6T full adder cell. The average leakage current of the proposed circuit is minimum as compared to all the full adder circuits except 7T_DPTL full adder cell.

TABLE 2
DC ANALYSIS RESULT OF DIFFERENT FULL ADDER CELLS @ V_{DD} = 0.9 V.

Full Adder Cell Designs ↓	Cout_HI (Min)	Cout_LO (Max)	Sum_HI (Min)	Sum_LO (Max)
6-T	0.742	0.157	0.817	0.153
7T_UB	0.817	0.1	0.77	0.1
7T_LDPTL	0.746	0.187	0.735	0
8T_BB	0.817	0.1	0.717	0
7T_DPTL	0.817	0.1	0.801	0.1
8T_DPTL	0.815	0	0.815	0.1

B. Static Power Analysis

Figure 5 shows the static power dissipation for different full adder cells for all 8 input combinations. The proposed design has the lowest leakage current as compared to other circuits in most of the input combinations. The average static power dissipation of the proposed circuit is minimum as compared to all the full adder circuits except 7T_DPTL full adder cell.

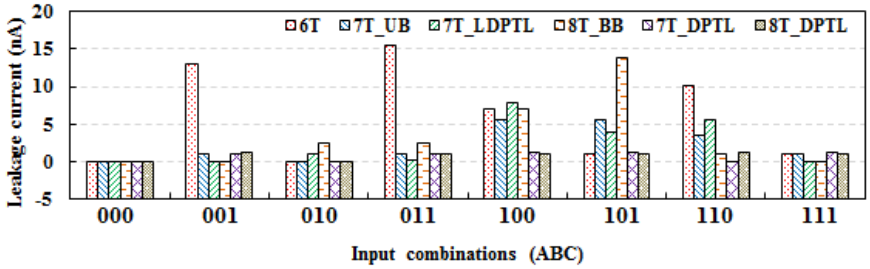

Figure 4: Leakage current of different FA cells for different input combinations.

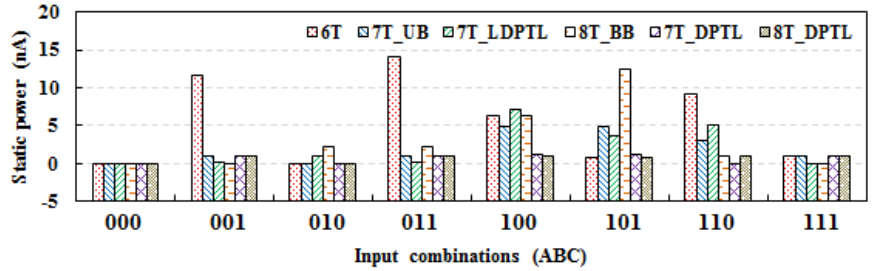

Figure 5: Static power dissipation of different FA cells for different input combinations.

C. Dynamic Power Analysis

Dynamic power is the power dissipation during the active period of the circuit means when there are transitions in the inputs. For simulation four different input frequencies 12.5 MHz, 25 MHz, 50 MHz, and 100 MHz have been considered. Figure 6 shows the dynamic power dissipation for different full adder cells at four input frequencies. From the results, we can observe that the dynamic power of circuit increases as input frequency increases. The dynamic power dissipation of 8T_DPTL full adder cell has the lowest power dissipation as compared to all other full adder cells at all four frequencies.

D. Delay Analysis

Delay of any circuit represents the speed of operation of the circuit. For high performance and high computing systems, the delay of the circuits should be as small as possible. Figure 7 shows the delay of different full adder cells, and it is observed that the proposed 8T_DPTL full adder cell is 58.7% faster as compared to 6T full adder cell. The 7T_DPTL full adder cell has the smallest delay as compared to all other cells and has 0.5% less delay compared to 8T_DPTL full adder cell.

E. Area Analysis

The optimum area of the circuit depends on the proper placing and routing of different components. For the optimum operation of IC, the placing of component and their interconnection with shortest path is required. In the absence of actual layout, the estimated area of all full adder cells has been calculated using transistor sizes. For calculation of the

approximate area of full adder cell, the product of length and width of each transistor in the cell is added together. The approximate area of the full adder can be calculated as:

$$Approximate\ Area \approx \sum_{k=1}^{n} W_k \times L_k$$

Where W and L are the width and length of the transistor respectively, and n is the number of transistors in the full adder cell. Figure 7 shows the estimated area for the different designs. The estimated area of 7T_UB full adder cell is smallest as compared to all other full adder cells. Even though the number of transistors increases by 2 in 8T_DPTL as compared to 6T full adder cell, the estimated area is less because of small sizing required in the 8T_DPTL full adder cell to achieve the better output levels.

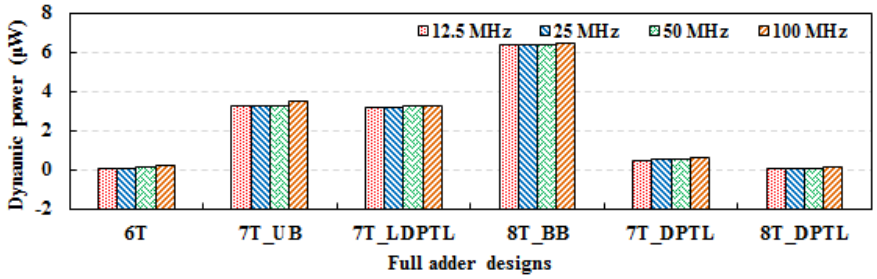

Figure 6: Dynamic power dissipation of different FA cells at different input frequencies.

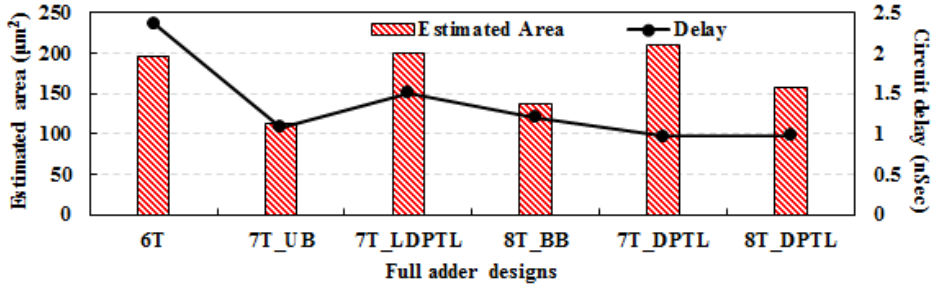

Figure 7: Approximate estimated area and worst-case circuit delay of different FA cells.

TABLE 3
NORMALIZED VALUES OF DIFFERENT STATIC AND DYNAMIC PARAMETERS FOR DIFFERENT FA CELLS.

Performance Parameters ↓	Full Adder Cell Designs ↓					
	6T	**7T_UB**	**7T_LDPTL**	**8T_BB**	**7T_DPTL**	**8T_DPTL**
Average leakage current (nA)	6.002	2.240	2.407	3.368	0.752	0.823
Normalized leakage current	**1**	**0.373**	**0.401**	**0.561**	**0.125**	**0.137**
Average static power (nW)	5.402	2.016	2.166	3.032	0.677	0.741
Normalized static power	**1**	**0.373**	**0.401**	**0.561**	**0.125**	**0.137**
Dynamic power at 100 MHz (µW)	0.184	3.451	3.282	6.414	0.630	0.156
Normalized dynamic power	**1**	**18.755**	**17.837**	**34.859**	**3.424**	**0.849**
Delay (nS)	2.368	1.086	1.508	1.201	0.967	0.978
Normalized delay	**1**	**0.459**	**0.637**	**0.507**	**0.408**	**0.413**
Estimated area (µm^2)	196.0	112.7	200.9	137.2	210.7	156.8
Normalized area	**1**	**0.575**	**1.025**	**0.700**	**1.075**	**0.8**
Figure of merit	**1**	**1.451**	**0.534**	**0.257**	**42.364**	**189.4**

F. Figure of Merit

A figure of merit (FOM) is a quantity which is used to characterize the performance of a circuit compared to its alternative circuits [12]. Lower the figure of merit better the performance of the circuit. FOM of full adder cell can be calculated as:

$$FOM = \frac{1}{I_{Norm} \times SP_{Norm} \times DP_{Norm} \times T_{Norm} \times A_{Norm}}$$

Where, I_{Norm}, SP_{Norm}, DP_{Norm}, T_{Norm}, and A_{Norm} are the normalized leakage current, static power, dynamic power, circuit delay and estimated area respectively. From Table 3, it is observed that the FOM of 8T_DPTL is very high as compared to all other circuits. The FOM of proposed full adder cell is 189.4 times better as compared to 6T full adder cell.

4. Conclusion

In this paper, a novel low power high speed 8 transistor one-bit full adder cell based on degenerate pass transistor logic is presented. Proposed 8T_DPTL full adder cell has better control in leakage current and static power dissipation as compared to all other full adder cells except 7T_DPTL whereas the dynamic power of 7T_DPTL is large as compared with 8T_DPTL. The dynamic power dissipation of proposed 8T_DPTL is minimum as compared to all other full adder cells. The circuit delay of the proposed cell is also less as compared to all other circuits. Even though the number of transistors required in the proposed circuit is increased by 2, the estimated area required is less as compared to 6T full adder cell because of increased sizing of the transistor to get the appropriate outputs. To analyze the quality of the circuit, FOM has been proposed. The FOM of the proposed cell has improvement with excellent margin hence proposed full adder cell is best suited for high performance and high-speed applications.

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Features

Reactive current compensation method for PFC applications based on SOGI-PLL

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Abstract – Power electronic devices typically use electromagnetic interference (EMI) filter and a power factor correction (PFC) stage. The EMI filter contains X-capacitors, which cause reactive currents. These decrease the devices power factor of the device, when working under light load conditions. These conditions are typically present at the end of battery charging. This paper introduces a new method for reactive current compensation for single PFC applications, based on a digital second order generalized integrator (SOGI) phase locked loop (PLL). This compensation method is able to improve the devices power factor under light load conditions significant. It is also possible to control the devices power factor to support advanced techniques like reactive of local grid infrastructure. Additionally a new design method based on the extended describing function method (EDF) for the proposed compensation method is shown in detail. Both methods are validated with a $3{,}6kW$ PFC boost converter.

1. Introduction

Most power electronic devices using a single PFC circuit for power factor correction. The PFC shall align the present grid voltage and the devices input current. This means the PFC circuit shapes the input current as the shape of the grid voltage. If the grid voltage and the input current are aligned, the reactive power losses decreasing. The alignment state is measured with the power factor and the total harmonic distortion (THD). Target of a PFC circuit is to keep the power factor as close to one as possible and keep the THD as low as possible. The general structure of a typical single PFC circuit is shown in Figure 1. On the left, the grid connection and EMI filter containing L1, L2, C1 and C2 is shown. The EMI filter output is connected to the digital controlled single phase PFC boost converter, containing a bridge rectifier, the inductance L3, a power mosfet and a power diode. [1] The PFC boost converter is controlled with a digital control algorithm, running on a microcontroller. Typically the grid voltage u_{AC} and the input current i_{AC} need to be measured as input signals for the control algorithm. But instead of u_{AC} and i_{AC} in most cases the voltage u_{PFC} and the current i_{PFC} behind the EMI filter are measured because of EMI restrictions. The EMI filter unfortunately contains capacitors and chokes, which are causing reactive power. This reactive power gets more noticeable during light loads conditions and is not measured by the PFCs voltage and current measurement. Because of this a standard PFC control algorithm is not able to compensate the EMI filters reactive power. [2] The proposed method based on a second order generalized integrator, allows compensating the influence of the EMI filter without deceasing the robustness of the PFC control algorithm. At first a review of the state of art SOGI-PLL method is given. After that the SOGI-PLL method is extended with the proposed method. Finally the performance of the extended PFC is verified.

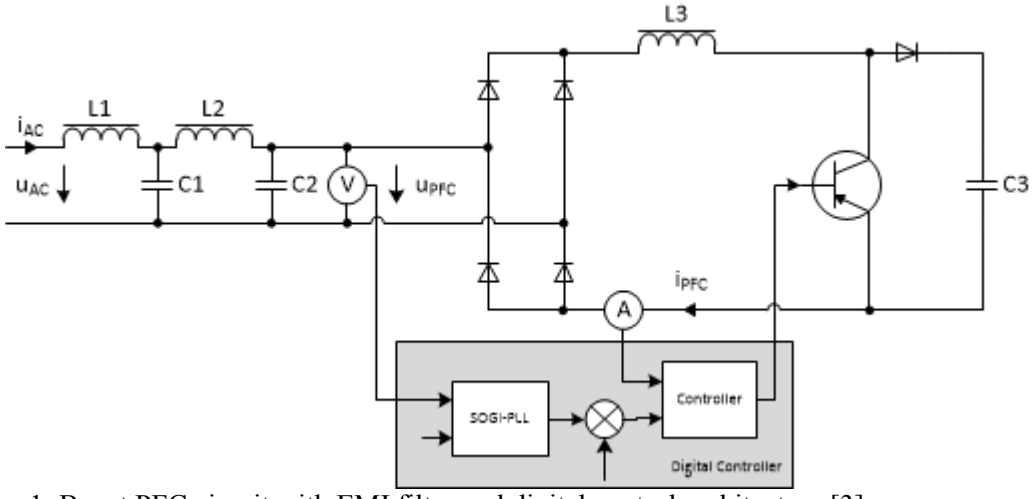

Figure 1: Boost PFC circuit with EMI filter and digital control architecture.[3]

2. State of Art SOGI-PLL

The digital SOGI-PLL is used in different applications [4] like photovoltaic inverters, battery chargers and other grid connected devices, to reach various targets, like grid voltage zero crossing detection, grid voltage filtering or frequency estimation. With a few extensions it can also be used for grid voltage harmonics analysis [5]. The digital SOGI can be represented as state space model.

$$\begin{pmatrix} \dot{x_1} \\ \dot{x_2} \end{pmatrix} = \begin{pmatrix} -b & -\omega \\ \omega & 0 \end{pmatrix} \begin{pmatrix} x_1 \\ x_2 \end{pmatrix} + \begin{pmatrix} b \\ 0 \end{pmatrix} u \qquad (1)$$

$$\begin{pmatrix} y_1 \\ y_2 \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \begin{pmatrix} y_1 \\ y_2 \end{pmatrix}$$

The angular frequency ω is the frequency, the filter is adapted to. The filter coefficient b defines the quality of the filter. A Bode plot of the input to output transfer function of the SOGI is shown in Figure 2 for different filter coefficients. The adapted frequency ωpasses the filter with zero phase deviation, while all other frequencies are damped. This makes the SOGI to an ideal bandpass filter in the input of a digital PFC control. The steepness of the resonance peak, and therefor the filter quality, can be controlled with the filter coefficient.

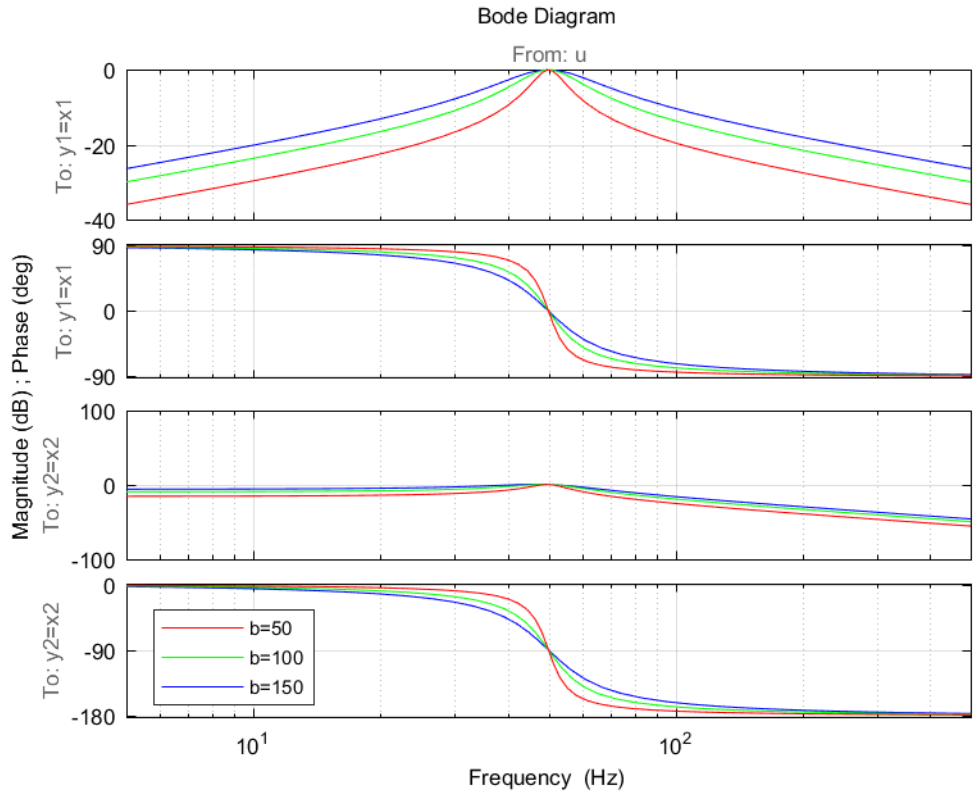

Figure 2: Continuous time transfer function bode plot of the SOGI for different filter coefficients b.

Without any further actions the SOGI filter is only able to adapt the first harmonics with the angular frequency ω. To expand the filter functionality to variable frequencies, a phase locked loop (PLL) is added. The PLL adapts the first harmonic frequency of the input signal u and passes it to the SOGI. Therefore the parameter ω in equation (1) is substituted by the PLL output a.

$$\begin{pmatrix}\dot{x_1}\\ \dot{x_2}\end{pmatrix} = \begin{pmatrix}-b & -a\\ a & 0\end{pmatrix}\begin{pmatrix}x_1\\ x_2\end{pmatrix} + \begin{pmatrix}b\\ 0\end{pmatrix}u \qquad \textbf{(2)}$$

$$\begin{pmatrix}y_1\\ y_2\end{pmatrix} = \begin{pmatrix}1 & 0\\ 0 & 1\end{pmatrix}\begin{pmatrix}y_1\\ y_2\end{pmatrix}$$

To find the required frequency a the PLL detects the current phase p based on the input signal u and both output signals y_1, y_2. The deviation of the detected phase from a given phase set point w is the currently existing control deviation. It is fed to an I-controller, which is creating the SOGI parameter a. This can be described by adding equations (4) and (5) to the SOGI description.

$$\begin{pmatrix}\dot{y_1}\\ \dot{y_2}\end{pmatrix} = \begin{pmatrix}-b & -a\\ a & 0\end{pmatrix}\begin{pmatrix}y_1\\ y_2\end{pmatrix} + \begin{pmatrix}b\\ 0\end{pmatrix}u \qquad \textbf{(3)}$$

$$p = (u - y_1)y_2 \qquad \textbf{(4)}$$

$$\dot{a} = a + k_i p \qquad \textbf{(5)}$$

Where k_i is the integral parameter of the I-controller. If the phase set point is zero, the PLL ensures, that the SOGI filter is always locked to the input signals base frequency $a = \omega$.

3. Mathematical modeling based on EDF

For designing the PLL parameter the input to output transfer function is required. In this section a new modeling method, based on the extended describing functions method, is shown. The EDF method is known from small signal modeling of LLC resonant switching converters [6],[7] and can be used for small signal modeling of the SOGI-PLL. Hence the system states y_1, y_2 from equation (3) can be represented by their sin and cos components.

$$\langle y_1 \rangle_1 = y_1 \sin(\omega t) + y_1 \cos(\omega t) \quad \textbf{(6)}$$

$$\langle y_2 \rangle_1 = y_2 \sin(\omega t) + y_2 \cos(\omega t) \quad \textbf{(7)}$$

This represents the first harmonic oscillation the SOGI filter can adapt. For output equation (4) only the DC component is required.

$\langle p \rangle_{DC} = \langle r p y_2 \rangle_{DC}$

$$\langle p \rangle_{DC} = \langle (u - y_1) y_2 \rangle_{DC} \quad \textbf{(8)}$$

Differentiating the equations (6) and (7) leads to representations for the left side of equation (3). With this the first EDF model equations can be found by substituting equations (6) and (7) into system equation (3). The resulting equations can be separated into their sin and cos components. This leads to four first order differential equations.

$$\dot{y}_{1S} = \omega y_{1C} - b y_{1S} - a Y_{2S} + b \bar{u} \quad \textbf{(9)}$$

$$\dot{y}_{1C} = -\omega y_{1S} - b y_{1C} - a y_{2C} \quad \textbf{(10)}$$

$$\dot{y}_{2S} = \omega y_{2C} + a y_{1S} \quad \textbf{(11)}$$

$$\dot{y}_{2C} = -\omega y_{2S} + a y_{1C} \quad \textbf{(12)}$$

The last EDF model equation is based on equation (4). Here only the DC components are required, which can be found by building the magnitudes of y_1, y_2 and u. The input value is the magnitude $\bar{u}$. The magnitudes of the system variables can be found by building the vector magnitude out of the sin and cos components.

$$|u| = \bar{u} \quad \textbf{(13)}$$

$$|y_1| = \sqrt{y_{1S}^2 + y_{1C}^2} \quad \textbf{(14)}$$

$$|y_2| = \sqrt{y_{2S}^2 + y_{2C}^2} \quad \textbf{(15)}$$

Inserting the magnitude equations into equation (4) leads to the last required equation of the PLL model.

$$\langle p \rangle_{DC} = \bar{u} y_{1C} \frac{\sqrt{y_{2S}^2 + y_{2C}^2}}{\sqrt{y_{1S}^2 + y_{1C}^2}} \quad \textbf{(16)}$$

Because of the nonlinear square root operation in equations (14) and (15) this is a nonlinear model. For designing the controller parameter of the PLL phase controller a linear model is required. The EDF model can be linearized by standard methods. Due to the fact, that the phase detection is build on a subtraction of the sinusoidal signals u and y_1 the phase signal will also be a sinusoidal function with the same frequency. The open loop transfer function should have a good damping at the input signal frequency and sufficient phase reserve at the crossover frequency. Figure 3 shows an open loop design for different filter coefficients b. Because the open loop transfer function differs for lower frequencies, the crossover frequency at the phase margin is depending on the filter parameter. This requires designing the SOGI filter before designing the PLL.

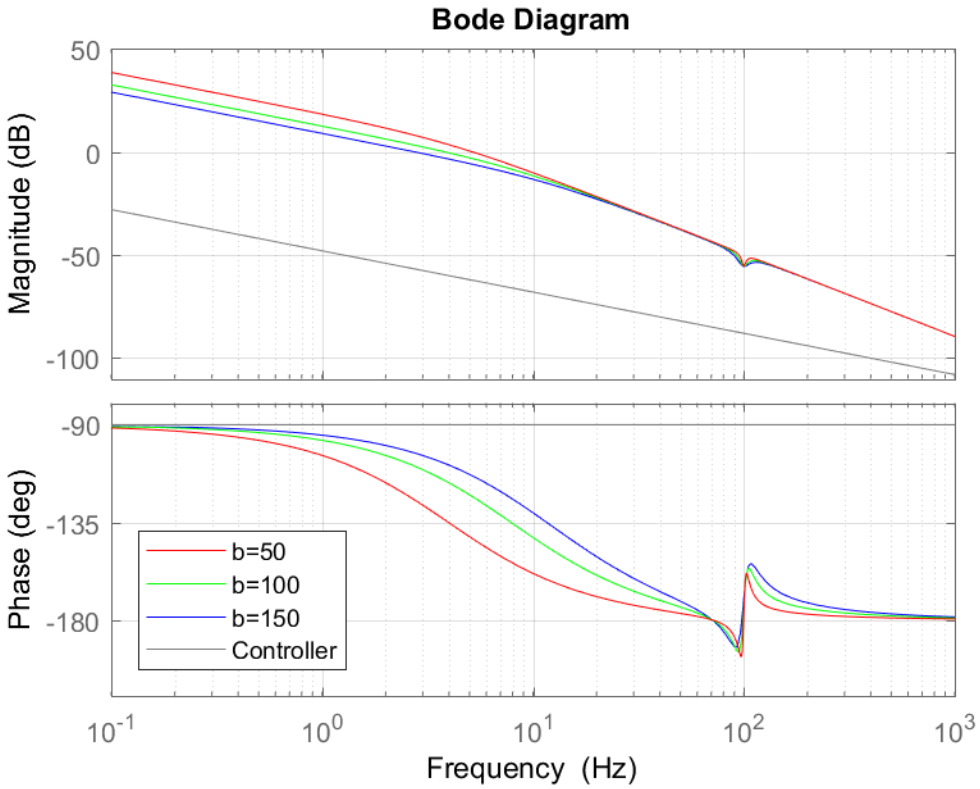

Figure 3: Continuous open loop control design of the PLL for different filter parameter.

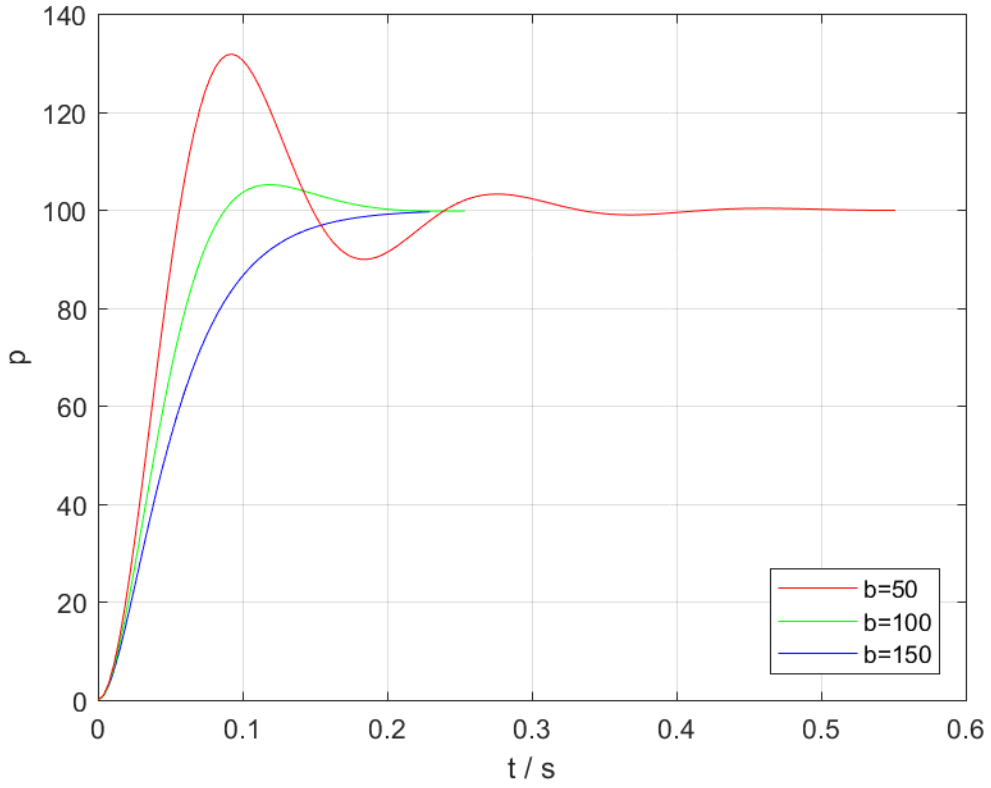

Figure 4: PLL step responses for different filter parameter.

Figure 4 shows the corresponding step responses of the PLL. The different crossover frequencies and phase margins cause different transient times and overshoots. Figure 5 shows a simulation of the SOGI-PLL for the filter parameter $b = 50$. The mean value of the phase measurement is equal to the proposed step response of the EDF model.

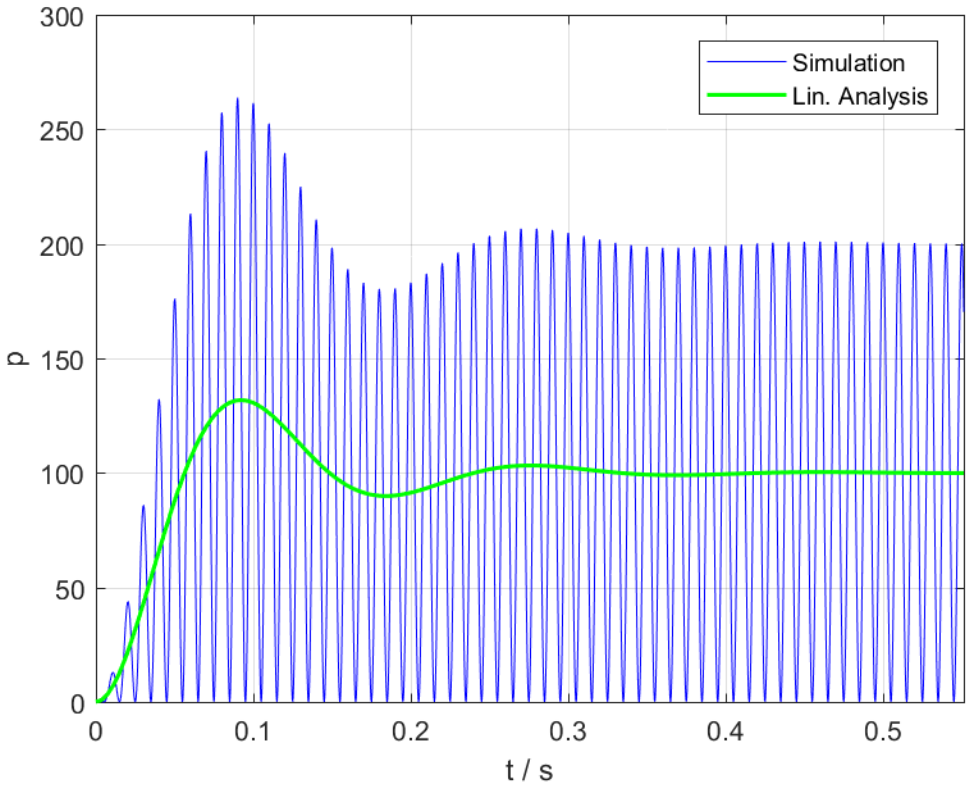

Figure 5: Step response compare between linear analysis result and simulation

4. Power Factor Improvements for PFC Applications

For a new method of input capacitor current compensation [2], the shown behavior of the SOGI-PLL can be used to improve the power factor of PFC applications at lower load conditions. Because in lower load conditions, the typically used input filters complex impedance causes a much higher phase deviation between the controlled PFC current and the grid input current measured at the devices input clamps. This can be calculated geometrically.

$$\tan(\Phi_0) = \frac{I_C - I_L}{I_{PFC}} \tag{17}$$

Were I_C and I_L are the rms currents caused by the filter components. The choke current i_L is compensating the much higher capacitor current i_C partly and is therefore subtracted. The phase deviation $\tan(\Phi_0)$ is getting smaller with higher PFC-current I_{PFC}. This explains the better power factor at higher load conditions. By knowing this, its possible to use the SOGI-PLL phase behavior shown in Figure 1 to compensate the power factor loss. At the frequency a the SOGI is adapted too, the phase of the output signal y1 is zero. If the frequency decreases the phase increase towards 90°, as the frequency increases, the phase is decreasing towards -90°. So the currents phase deviation can be compensated by tuning the SOGI towards a lower parameter a, which will increase the phase of the output y_1. This results in a delayed SOGI output y_1 and therefore to a delayed current setpoint for the PFC's current controller. The phase deviation of the SOGI can be calculated by creating the transfer function of the first output from the state space model (2) and splitting it into real and imaginary parts.

$$G_{y_1} = \frac{j\omega b}{(j\omega)^2 + j\omega b + a^2}$$

$$G_{y_1} = \frac{(j\omega b)\left((a^2 - \omega^2) + j\omega b\right)}{\left((a^2 - \omega^2) + j\omega b\right)^2}$$

$$Re\left(G_{y_1}\right) = \frac{b^2}{\left(\frac{a^2}{\omega}\right)^2 - 2a^2 + \omega^2 + b^2} \quad \textbf{(18)}$$

$$Im\left(G_{y_1}\right) = \frac{b\frac{a^2}{\omega} - b\omega}{\left(\frac{a^2}{\omega}\right)^2 - 2a^2 + \omega^2 + b^2} \quad \textbf{(19)}$$

To compensate the filters phase deviation, the phase deviation $\Delta\Phi$ of the SOGI shall be exactly the opposite of the input currents phase deviation Φ_0 caused by the input filter. The connection between them can be found easily with equation (17) and the calculated transfer functions (18), (19).

$$\tan(\Delta\Phi) = \frac{Im(G_{y_1})}{Re(G_{y_1})} = -\tan(\Phi_0) \quad \textbf{(20)}$$

$$\frac{\frac{a^2 - \omega}{\omega} - \omega}{b} = \frac{I_C - I_L}{I_{PFC}}$$

$$a = \sqrt{\left(\frac{I_C - I_L}{I_{PFC}} b + \omega\right)\omega} \quad \textbf{(21)}$$

With equation (21) it is possible to calculate the required SOGI parameter a. Next a connection between the PLLs phase setpoint w and the SOGIs phase deviation $\Delta\Phi$ is required. This can be derived from the SOGIs DC gains G. [8] They can be calculated by solving the independent state transfer functions for the EDF model differential state equations (9), (10), (11) and (12).

$$G_p(\Delta\Phi) = G_{1C}(\Delta\Phi)\frac{\sqrt{G_{2S}(\Delta\Phi)^2 + G_{2C}(\Delta\Phi)^2}}{\sqrt{G_{1S}(\Delta\Phi)^2 + G_{1C}(\Delta\Phi)^2}} \quad \textbf{(22)}$$

The gain $G_p(\Delta\Phi)$ is the normalized gain of the SOGI-PLL system. By applying it to the last EDF state equation (16) the required connection can be found.

$$\langle p \rangle_{DC} = \bar{u}^2 G_p(\Delta\Phi) \quad \textbf{(23)}$$

The input $\bar{u}$ appears doubled in this equation, as in the real system it is for sure also part of the systems response. It can be used together with equation (20) to calculate the required phase setpoint w.

$$w = \bar{u}^2 G_p(\Delta\Phi)\Delta\Phi \quad \textbf{(24)}$$

5. Experimental Verification with Boost PFC

G_p is plotted in Figure 6 over the phase target $\Delta\Phi$. In single phase PFC applications it is not possible to correct the total phase at all times. This is caused by the rectifier inside the PFC converters input circuit. Therefor it is only possible to correct the phase in a range of 0° to 20°. This matches with the SOGI-PLL which is also only able to shift the phase between $-30°$ to 40°. This is results due to the plotted gain contains a maximum and a minimum. If they are exceeded, the PLL becomes instable.

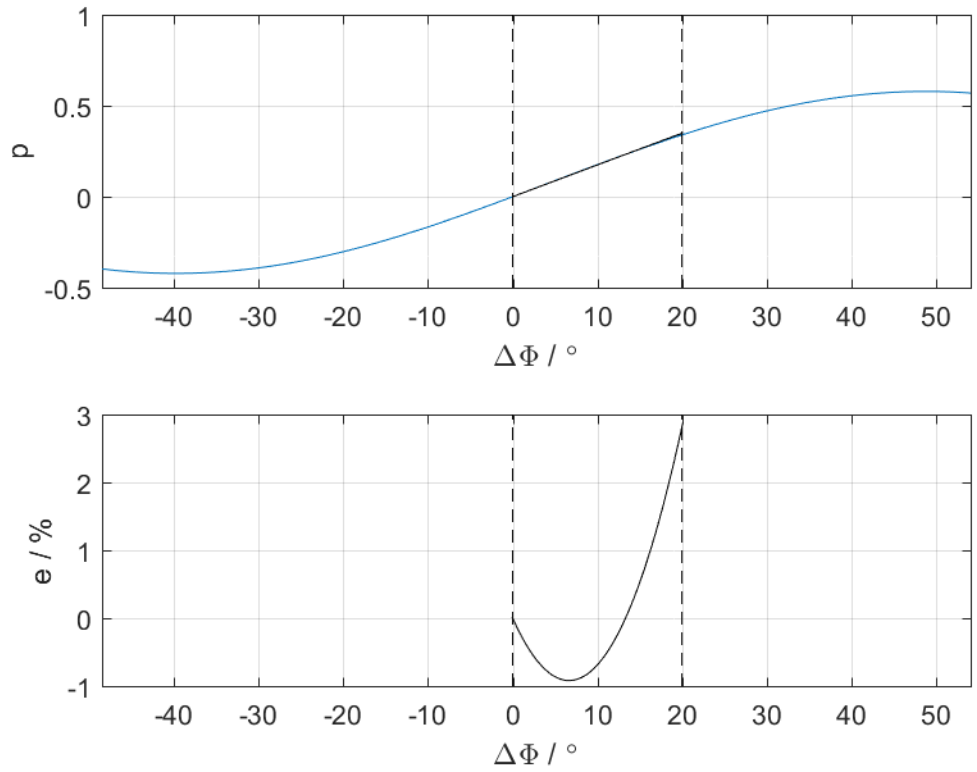

Figure 6: Plot of the phase detection in blue and linear approximation in black in the first inset and the approximation error in the second one.

Over to this results phase correction should focus on the nearly linear region between 0° to 20°, marked between the both dotted lines in Figure 6. This nearly linear region is existent because of the transfer function properties of the SOGI. The region can also be seen in the phase curve of y_1 plotted in Figure 1. As shown in equation (22) the calculation of $G_p(\Delta\Phi)$ is complicated and should not be done online on a typically used low power processor. Because of this an approximation is required. It is possible to apply a correction factor f_C if a correction of $-30°$ to 30° is required. The general equations (24) and (17) can be approximately rewritten.

$\omega = \bar{u}^2 f_C \Delta\Phi$

$$\omega = \bar{u}^2 f_C \arctan\left(\frac{I_C - I_L}{I_{PFC}}\right) \tag{25}$$

For small corrections between 0° to 20° it can be assumed that f_C is equal to 1. This will cause an approximation error which is shown in the second inset of Figure 6 for the relevant region. The approximation error reaches only 3%. The simplified equation (25) can be easily integrated into available digital signal processors. The correction has been tested with a 3,6kW single phase boost PFC. The result is shown in Figure 7. The blue line shows the achieved power factor over load with active reactive current compensation, the red line with offline reactive current compensation. As proposed, the power factor with active compensation is much better in light load conditions as the one with no compensation. Without further hardware improvements a much better compensation is not possible without highly improving the THD. This is because of the in Figure 1 shown bridge rectifier inside the PFC circuit. For better compensation a bi directional PFC circuit is required [3]. For one directional PFC circuits this method allows to compensate the power factor under light load conditions as best as possible.

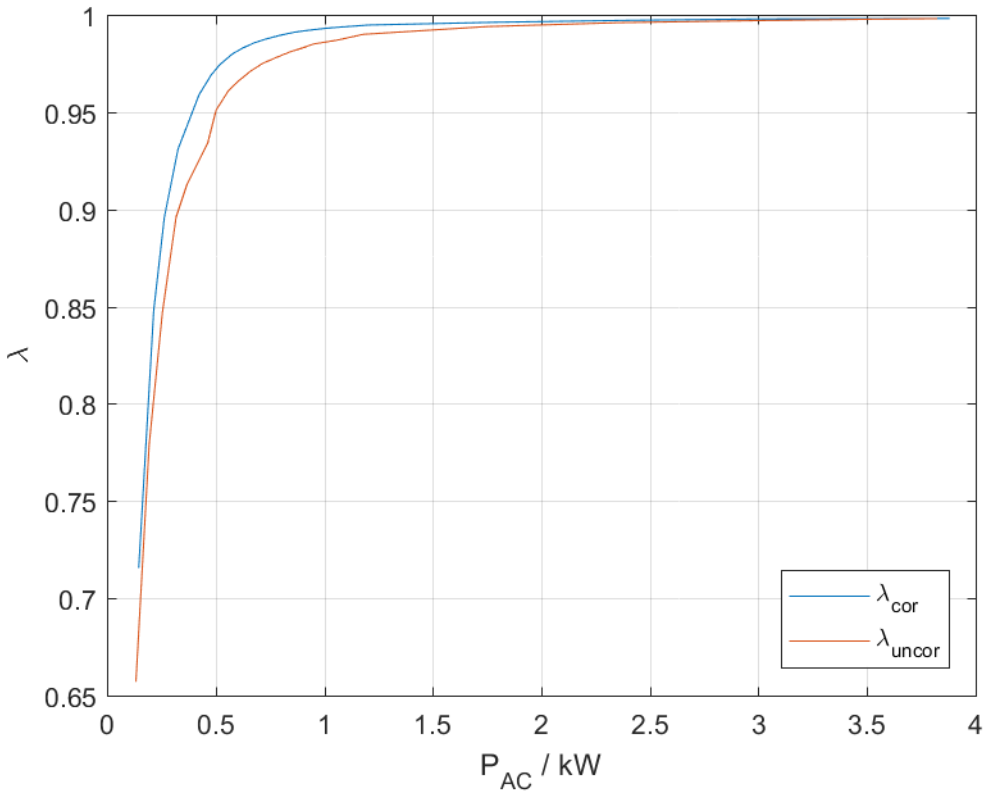

Figure 7: Measured power factor with activated correction in blue and deactivated correction in red.

The proposed compensation method also allows to control the reactive power to a defined setpoint, by using the input w. Therefor the power setpoint Φ_{Target} can be added it to equation (25).

$$\omega = \bar{u}^2 f_C \arctan\left(\frac{I_C - I_L}{I_{PFC}} + \Phi_{Target}\right) \quad \textbf{(26)}$$

This allows the one directional single PFC circuit to control the devices reactive power for example in a range of $-30°$ to $30°$. Which would make every device using this method to a smart grid device, that can be used to compensate grids phase relation at every grid region the device is connected to.

6. Conclusion

In this paper a new method for reactive current compensation based on the SOGI-PLL has been proposed. Additional a design method based on three steps has been shown:

- Design of the SOGI filter quality by defining the quality factor b.
- Design of the PLL by defining the phase controllers integral part k_i.
- Design of the reactive current compensation by defining the approximation factor f_C

With this method an example system based on a 3,6kW single phase boost PFC has been designed and tested. The system was able to compensate the reactive current up to an phase delay of 20°. This leads to a significant power factor improvement at light load conditions compared to a state of the art PFC without reactive power compensation. It also has shown, that it is possible to shift the phases in negative directions which is an interesting ability in the context of smart grid applications. If this solution is implemented in chargers for electric cars it is possible to correct grids total phase in the nearby regions.

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Title	Program Guidelines	Due Dates
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Mid-scale Research Infrastructure-2 (Mid-scale RI-2) N NSF-wide	19-542	Full Proposal: August 2, 2019
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Research Experiences for Undergraduates (REU) N NSF-wide	13-542	Full Proposal: August 28, 2019
Historically Black Colleges and Universities Undergraduate Program (HBCU-UP)	18-522	Letter of Intent: September 3, 2019
Smart and Connected Communities (S&CC)	19-564	Full Proposal: September 6, 2019
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Information and Intelligent Systems (IIS): Core Programs	18-570	Full Proposal: September 25, 2019
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Computing and Communication Foundations (CCF): Core Programs	18-568	Full Proposal: November 14, 2019
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Collaborative Research in Computational Neuroscience (CRCNS)	18-591	Full Proposal: November 25, 2019
Historically Black Colleges and Universities Undergraduate Program (HBCU-UP)	18-522	Full Proposal: November 26, 2019
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Small Business Technology Transfer Program Phase I (STTR) N NSF-wide	19-555	Full Proposal: December 12, 2019
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Computing Job Announcements – CRA	https://cra.org/ads/
PolytechnicPositions	www.polytechnicpositions.com/

Upcoming Conferences/Workshops

- ✓ IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC), Hirosaki, Japan, May 12-15, 2019; web: http://www.async2019.jp

- ✓ International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, May 26-29, 2019; web: https://www.iscas2019.org

- ✓ The 24th IEEE European Test Symposium (ETS), Baden-Baden, Germany, May 27-31, 2019; web: https://www.testgroup.polito.it/ets19/

- ✓ IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Boston, Massachusetts, USA, June 2-4, 2019; web: https://rfic-ieee.org

- ✓ ACM/IEEE System Level Interconnect Prediction (SLIP), Las Vegas, NV, USA, June 2, 2019; web: http://www.sliponline.org

- ✓ Design Automation Conference (DAC), Las Vegas, NV, USA, June 2-6, 2019; web: https://dac.com/

- ✓ Symposia on VLSI Technology and Circuits (VLSI), Kyoto, Japan, June 9-14, 2019; web: http://vlsisymposium.org

- ✓ IEEE Symposium on Computer Arithmetic (ARITH), Kyoto, Japan, June 10-12, 2019; web: http://www.lab3.kuis.kyoto-u.ac.jp/arith26/

- ✓ International Workshop on Logic & Synthesis (IWLS), Lausanne, Switzerland, June 21-23, 2019; web: http://www.iwls.org/iwls2019/

- ✓ International Conference on Application of Concurrency to System Design (ACSD), Aachen, Germany, June 23-28, 2019; web: http://www.petrinets2019.de/acsd-2019/

- ✓ IEEE International Workshop of Electronics, Control, Measurement, Signals and their application to Mechatronics (ECMSM), Toulouse, France, June 24-26, 2019; web: http://www.ecmsm2019.com

- ✓ IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), Cornell Tech, New York, USA, July 15-17, 2019; web: https://asap2019.csl.cornell.edu/

- ✓ IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Miami, Florida, USA, July 15-17, 2019; web: http://www.isvlsi.org

- ✓ European Solid-State Circuits Conference (ESSCIRC) / European Solid-State Device Research Conference (ESSDERC), Krakow, Poland, September 23-26, 2019; web: https://esscirc-essderc2019.org

- ✓ IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Cuzco, Peru, October 6-9, 2019; web: https://vlsi-soc.pe

- ✓ The 52nd IEEE/ACM International Symposium on Microarchitecture (MICRO), Columbus, Ohio, USA, October 12-16, 2019; web: https://www.microarch.org/micro52/

- ✓ Embedded Systems Week (ESWEEK), New York, USA, October 13-18, 2019; web: https://www.esweek.org/

- ✓ IEEE Asian Solid-State Circuits Conference (A-SSCC), Macao, China, November 4-6, 2019; web: http://www.a-sscc2019.org/

- ✓ International Conference on Computer Aided Design (ICCAD), Westminster, CO, USA, November 4-7, 2019; web: https://iccad.com/

- ✓ IEEE International Conference on Computer Design (ICCD), Abu Dhabi, United Arab Emirates, November 17-20, 2019; web: https://www.iccd-conf.com/Home.html

- ✓ IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Bangkok, Thailand, November 25-28, 2019; web: http://www.apccas2019.org

IEEE Computer Society

Technical Committee on VLSI

Post-Conference Report - TCVLSI Technically Co-Sponsored Conferences (Nov. 2018 to Mar. 2019)

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1. **IEEE International Symposium on Smart Electronic Systems (IEEE-iSES, formerly IEEE-iNIS), December 17-19, 2018, Hyderabad, India:**

IEEE-iSES 2019 hosted 3 keynote talks, i.e., (1) "Sensor platforms for providing affordable IoT solutions to the developing world" given by V. Ramgopal Rao from Indian Institute of Technology (IIT) Delhi, (2) "Smart electronic systems" given by Saraju P. Mohanty from University of North Texas, USA, and (3) "Architecting Internet-of-Things systems: impending challenges and integrative solutions" given by Dr. Sandip Ray from University of Florida, USA. It organized 19 sessions, i.e., (1) Memory & arithmetic circuits, (2) VLSI and security, (3) Microhotplate: modelling and validation, (4) Multi-processors, (5) Placement and application mapping, (6) FPGA design & arithmetic circuits, (7) Analog design, (8) Memory and approximate computing, (9) Sensing and wireless IoT, (10) Secure MANET and smart system, (11) IoT data analytics and memory overflow, (12) Energy harvesting and IoT, (13) Emerging designs and fabrication, (14) IoT and vehicular security, (15) Smart systems and design for IoT, (16) IoT and smart city, (17) Bio-sensing and Biometric systems, (18) Cybersecurity, and (19) Embedded and ad-hoc network. It also organized 5 special sessions, i.e., (1) Energy recovery and DSP cores, (2) IoT and smart health, (3) Systems for smart healthcare, (4) FPGA designs for innovative on-chip communication solutions, and (5) Big Data and IoT for societal issues in India.

The **General Chairs** of IEEE-iSES 2019 were M. B Srinivas from BML Munjal University, India and Sudeep Pasricha from Colorado State University, USA. The **Program Chairs** were Himanshu Thapliyal from University of Kentucky, USA and Marina Gavrilova from University of Calgary, Canada.

2. **International Conference on VLSI Design (VLSID), January 5-9, 2019, Manekshaw Centre, New Delhi, India:**

VLSID 2019 organized 12 tutorials, i.e., (1) "The autonomous automotive robustness duo: challenges and practice in functional safety and security" given by Prof. Sandip Ray from University of Florida, USA, (2) "Designing in the next generation IoT-AI ecosystem" given by Dr. Manish Sharma and Mahesh Babu A. K. from Samsung, (3) "Architecture and circuits for fractional-N clock synthesis in wireline/wireless applications" given by Prof. Saurabh Saxena and Prof. Nagendra Krishnapura from IIT Madras, (4) "Architecture & Methodology for DFT of Low Power SoCs" given by Jais Abraham and Arvind Jain from Qualcomm, (5) "Logic locking: current trends, attacks and future directions" given by Prof. Ujjwal Guin from Auburn University, USA, and Prof. Pramod Subramanyan from IIT Kanpur, (6) "The black art of analog design and validation: where search and optimization meet" given by Prof. Shobha Vasudevan from University of Illinois at Urbana Champaign, USA, (7) "Accelerating deep learning

inference on FPGAs using OpenVINO given by Vikas Hosoor from Intel, (8) “Offset in low-voltage sense amplifiers and its implication on memory testing” given by Prof. Manoj Sachdev from University of Waterloo, Canada, (9) “Vision based autonomous systems” given by Prof. Subhashis Banerjee and Prof. Chetan Arora from IIT Delhi, (10) “Hardware security of embedded systems and IoT environment” given by Prof. Susmita Sur-Kolay from ISI, Kolkata and Prof. Debasri Saha from University of Calcutta, (11) “Energy-efficient resilience for cognitive systems” given by Dr. Pradip Bose from IBM and Prof. Subhasish Mitra from Stanford, USA, and (12) “IoT for smarter healthcare: from device to architecture, applications and analytics” given by Prof. Nikil Dutt from University of California, Irvine and Iman Azimi from University of Turku, Finland.

It hosted 10 keynote talks, i.e., (1) “Semiconductors for the connected world-safe, secure, smart” given by Meindert Van Den Beld from NXP Semiconductor, (2) “Computational self-awareness: a paradigm for adaptive, resilient cyber-physical systems” given by Nikil Dutt from University of California, Irvine, (3) “Defining superior user experience in next gen connected world” given by Srini Maddali from Qualcomm India, (4) “Computing for the data-centric era” given by Dheemanth Nagaraj from Intel India Design Center, (5) “CONIX: computing on network infrastructure for new generation of cyber-physical systems and applications” given by Rajesh Gupta from University of California, San Diego, (6) “Smarter verification-beyond brute force” given by Alok Jain from Cadence Design Systems, (7) “Re-engineering computing with neuro-inspired learning: devices, circuits, and systems” given by Kaushik Roy from Purdue University, (8) “In memory compute-technology architecture confluence” given by Vijaykrishnan Narayanan from Pennsylvania State University, (9) “Nextgen innovations opportunities” given by Sanjay Gupta from NXP Semiconductor, and (10) “Enabling the data driven economy” given by Jaswinder Ahuja from Cadence Design Systems.

VLSID 2019 covered 11 tracks (i.e., (1) embedded systems, (2) analog/mixed signal, (3) digital design, (4) security, (5) test and validation, (6) test and validation, (7) CMOS devices (8) emerging tech (9) intelligence on silicon, (10) design automation, and (11) IoT and CPS) and organized 6 panels (i.e., (1) semiconductor Startups in India - a pipe dream, (2) autonomous intelligence for a safe, secure and smart world, (3) start up to scale up in IoT; from proof of concept to Production, (4) women in engineering - be the change, (5) hardware and security-opportunities & risks, and (6) academia-industry collaboration: challenges in the research pipeline). It also hosted two forums (i.e., industry forum and women in engineering forum) and two poster sessions, one for Ph.D forum and one for interactive presentation.

The **General Chairs** of VLSID 2019 were Preet Yadav from Wipro and Preeti Ranjan Panda from IIT-Delhi. The **Technical Program Chairs** were Jayadeva from IIT-Delhi and Prabhat Mishra from University of Florida.

CONTACT: TCVLSI CHAIR | ASENGUPT@IITI.AC.IN 2018

Technical Committee on VLSI (TCVLSI), IEEE-CS

http://www.ieee-tcvlsi.org

What is TC-VLSI?

A technical committee of IEEE-CS serves as the focal point of the various technical activities within a technical discipline.

TCVLSI is a constituency of the IEEE-CS that oversees various technical activities related to VLSI.

Key People

TCVLSI Chair
Anirban Sengupta, Indian Institute of Technology Indore
Newsletter EiC –
Anirban Sengupta, Indian Institute of Technology Indore
Vice Chair for Conferences –
Jia Di, University of Arkansas
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Hai (Helen) Li, Duke University
Vice Chair for Membership and Co-Webmaster – –
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Mike Borowczak, University of Wyoming
Past Chair –
Saraju Mohanty, University of North Texas, USA
Joseph Cavallaro, Rice University
Past Newsletter Co-EiC –
Saraju P. Mohanty, University of North Texas

TCVLSI Sister Conferences

Sponsored

ARITH: www.arithsymposium.org
ASAP: http://www.asapconference.org/
ASYNC: http://asyncsymposium.org/
iSES: http://www.ieee-ises.org (formerly iNIS)
ISVLSI: http://www.isvlsi.org
IWLS: http://www.iwls.org
MSE: http://www.mseconference.org
SLIP: http://www.sliponline.org
ECMSM: http://ecmsm2017.mondragon.edu/en

Technically Co-Sponsored

ACSD: http://pn2017.unizar.es/
VLSID: http://vlsidesignconference.org

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Technical Scope Various aspects of VLSI design including design of system-level, logic-level, and circuit-level, and semiconductor processes

TCVLSI Offers

- Student travel grants
- Best paper awards
- Timely CFP info
- Free membership
- Venue to contribute to VLSI
- Circuits & Systems Letter
- News & View to VLSI Community

IEEE VLSI Circuits & Systems Letter

IEEE Computer Society Technical Committee on VLSI
(A Quarterly Publication of IEEE-CS TC on VLSI, TCVLSI)

Aim and Scope

The IEEE VLSI Circuits and Systems Letter (VCAL) is a quarterly publication which aims to provide timely updates on technologies, educations and opportunities related to VLSI circuits and systems. The letter is published four times a year and it contains the following sections:

Features: selective research papers within the technical scope of TCVLSI. Goal is to report novel interesting topics related to TCVLSI, as well as short review/survey papers on emerging topics in the areas of VLSI circuits and systems.

Opinions: Discussions and book reviews on recent VLSI/nanoelectronic/emerging circuits and systems for nano computing, and "Expert Talks" to include the interviews of eminent experts for their concerns and predictions on cutting-edge technologies.

Updates: Upcoming conferences/workshops of interest to TCVLSI members, call for papers of conferences and journals for TCVLSI members, funding opportunities and job openings in academia or industry relevant to TCVLSI members, and TCVLSI member news.

Outreach and Community: The "Outreach K20" section highlights integrating VLSI computing concepts with activities for K-4, 4-8, 9-12 and/or undergraduate students.

Have questions on submissions; contact EiC: Dr. Anirban Sengupta (asengupt@iiti.ac.in)

Join TCVLSI for FREE to be a part of a global community, visit: http://www.ieee-tcvlsi.org

More information at:
https://www.computer.org/web/tcvlsi/circuits-and-systems-letter

Submission details:
Please visit the website and use standard VCAL template to prepare the manuscript

IEEE computer society

The IEEE Computer Society Technical Committee on VLSI

ISVLSI 2018

Students Travel Support Awards

Alireza Mahzoon, University of Bremen, mahzoon@informatik.uni-bremen.de
Leslie Hwang, University of Illinois at Urbana-Champaign, lkhwang@illinois.edu
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Zhiming Zhang, University of New Hampshire, zz1017@wildcats.unh.edu

JOIN The IEEE Consumer Electronics Society

Entertainment, Communications, Information,
Home Automation, Health Care, Education, Convenience
to name just a few focal points and growing each year

Why Join

Today's consumer electronics industry goes beyond legacy audio and video to now draw upon every field of electronics, communications, and information technology. We not only lead the state of the art in performance features and functions but our industry creates affordable products with the most advanced easy to use human factors. CESoc and the technologies we showcase in our publications, conferences, and local chapter meetings is the place to be to stay up to date on today's key technologies and tomarrow's emerging technologies.

Who is CESoc?

The field of interest of the Consumer Electronics Society is engineering and research aspects of the theory, design, construction, manufacture or end use of mass market electronics, systems, software and services for consumers. The society sponsors multiple conferences annually including the International Conference on Consumer Electronics and the International Symposium on Consumer Electronics

.

CESoc Membership includes

Monthly Society newsletter (electronic), Bi-Monthly IEEE Consumer Electronics Magazine (electronic and print), Quarterly IEEE Transactions on Consumer Electronics (electronic), IEEE Electrification Magazine (digital), Discounts on Conference Registration, Reduced Prices on Affiliated Journals, IEEE Consumer Electronics Society Digital Library (electronic) and IEEE Consumer Electronics Society Resource Center (electronic).

IEEE Membership Includes

Subscription to IEEE Spectrum magazine, The Institute and other relevant newsletters, electronic access to IEEE Potentials, IEEE Collabratec, inclusion in the IEEE Member Directory, members-only IEEE.tv programming, an exclusive ieee.org email account, discounts on products and services, continuing education, philanthropic opportunities, and more. Plus, you are automatically a part of your local IEEE Section and will receive communications about local networking opportunities, meetings, and special events.

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IEEE Transactions on Nanotechnology (TNANO) Special Section/Issue on the 18th IEEE International Conference on Nanotechnology (IEEE-NANO 2018)

Nanoscience and nanotechnology have rapidly established themselves as enabling disciplines within many disciplines including materials science, engineering, physics, chemistry, and biology. Following the success of the 18th IEEE International Conference on Nanotechnology (IEEE-NANO2018), IEEE Transactions on Nanotechnology (TNANO) is extending a Call For Papers for a Special Section /Issue reflecting the scope of the conference. Submitted manuscripts will undergo a full peer review process. Submissions are welcome but limited to NANO presentations. Authors who are attendees are requested to significantly expand the previous conference version to contain substantial new technical material, as per TNANO and IEEE restrictions on duplicated publications and the competitive acceptance process. Manuscripts for the TNANO Special Issue/Section must be submitted on-line using the IEEE TNANO manuscript template and "Information for Authors", via the IEEE Manuscript Central found at https://mc.manuscriptcentral.com/tnano. On submission to TNANO, authors should select the "Special Issue" manuscript type instead of "Regular Paper."

Submissions that reflect the Conference Scope and current state of the field are welcome in areas including:

- Micro-to- nano-scale bridging
- Nanobiology and Nanomedicine
- Nanoelectronics
- Nanomanufacturing and Nanofabrication
- Nano Robotics and Automation
- Nanomaterials
- Nano-optics, Nano-optoelectronics, and Nanophotonics
- Nanopackaging
- Nanoscale Metrology and Characterization
- Nanofluidics
- Nanomagnetics
- Nano/Molecular Heat Transfer & Energy Conversion
- Nano/Molecular Sensors, Actuators, and Systems
- Nanotechnology Safety, Education and Commercialization

Important Dates

- Submission of papers: **1 December, 2018**
- Notification of first review results: **1 March, 2019**
- Submission of revised papers: **15 April, 2019**
- Notification of final review results: **15 May, 2019**.

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems

Special Issue on

Hardware Oriented Security and Trust: Threats, Countermeasures and Design Tools

Call for Papers

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) is announcing a special issue on "*Hardware Oriented Security and Trust: Threats, Countermeasures and Design Tools*", which invites top papers accepted to the **2019 Asian Hardware Oriented Security and Trust Symposium (AsianHOST 2019**, http://asianhost.org/2019/**)** for extension and also calls for original research papers through public contributions.

The purpose of this special issue is to provide the targeted readers with the new advances and challenges in hardware security research and development. Topics of interest include discoveries of emerging security threats that are encountered by the hardware design and supply chain, demonstration of the most recent hardware security attacks and mitigations, as well as new security protection techniques and design methodologies that help to thwart these threats. Relevant topics include, but are not limited to, the following:

• Architectural and micro-architectural attacks and defenses
• Secure system-on-chip (SoC) architectures
• Side-channel attacks and countermeasures
• Hardware Trojan attacks and detection techniques
• IP core protection for consumer electronics systems and IoT
• Security and trust of machine learning and artificial intelligence
• Automobile, self-drive and autonomous vehicle security
• 5G, physical layer and wireless security
• Hardware-assisted cross-layer security
• Cyber-physical system (CPS) security
• Metrics, policies, and standards related to hardware security
• Security verification at IP, IC, and system levels
• Hardware IP trust (watermarking, fingerprinting, metering, trust verification)
• Reverse engineering and hardware obfuscation
• Supply chain risks mitigation including counterfeit detection & avoidance

• Trusted manufacturing including split manufacturing, 2.5D, and 3D ICs
• Emerging nanoscale technologies in hardware security applications
• Emerging nanoscale technologies in hardware security applications
• Hardware-intrinsic security primitives (Physical unclonable functions, true random number generator, etc.)
• Trusted platform modules and hardware virtualization

Paper Submission

All submissions must be made through the IEEE TCAD online paper submission system at https://mc.manuscriptcentral.com/tcad. Detailed submission instructions can be found at https://ieee-ceda.org/publication/tcad-publication/tcad-paper-submission

Submission Deadline: **March 1st, 2020**

Guest Editors

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IP Core Protection and Hardware-Assisted Security for Consumer Electronics

IP Core Protection and Hardware-Assisted Security for Consumer Electronics presents established and novel solutions for security and protection problems related to IP cores (especially those based on DSP/multimedia applications) in consumer electronics. The topic is important to researchers in various areas of specialization, encompassing overlapping topics such as EDA-CAD, hardware design security, VLSI design, IP core protection, optimization using evolutionary computing, system-on-chip design and application specific processor/hardware accelerator design.

The book begins by introducing the concepts of security, privacy and IP protection in information systems. Later chapters focus specifically on hardware-assisted IP security in consumer electronics, with coverage including essential topics such as hardware Trojan security, robust watermarking, fingerprinting, structural and functional obfuscation, encryption, IoT security, forensic engineering based protection, JPEG obfuscation design, hardware assisted media protection, PUF and side-channel attack resistance.

About the Authors

Anirban Sengupta is an Associate Professor in the Discipline of Computer Science and Engineering at Indian Institute of Technology (IIT) Indore. He has authored more than 182 publications and patents. His is recipient of several awards/honors such as IEEE Distinguished Lecturer, Outstanding Editor Award, IEEE CESoc Best Research Award from CEM, Best Research paper Award in IEEE ICCE 2019, IEEE Computer Society TCVLSI Outstanding Editor Award in 2017 and IEEE TCVLSI Best Paper Award in IEEE iNIS 2017. He holds 12 Editorial positions in Journals. He is the Editor-in-Chief of IEEE VCAL (Computer Society TCVLSI), and General Chair of 37th IEEE Int'l Conference on Consumer Electronics (ICCE) 2019, Las Vegas.

Saraju P. Mohanty is a tenured full Professor at the University of North Texas (UNT) where he directs the "Smart Electronic Systems (SESL)". He has authored 280 research articles, 3 books, and invented 4 US patents. He has received various awards and honors, including IEEE-CS-TCVLSI Distinguished Leadership Award in 2018, IEEE Distinguished Lecturer by the Consumer Electronics Society (CESoc) in 2017, PROSE Award for best Textbook in Physical Sciences & Mathematics in 2016, and 2016-17 UNT Toulouse Scholars award. He is the Editor-in-Chief of the IEEE Consumer Electronics Magazine (CEM). He serves as the Chair of Technical Committee on VLSI, IEEE Computer Society. He has received 4 best paper awards and has delivered multiple keynote talks at various International Conferences.

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Anirban Sengupta and Saraju P. Mohanty