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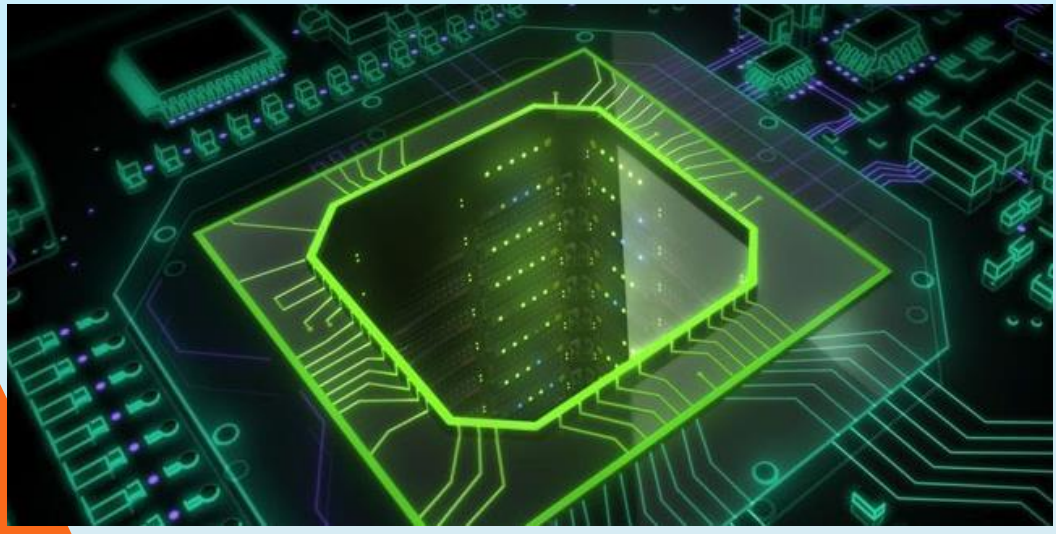
VLSI INTERCONNECTS



DELAY, AREA, POWER

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VLSI Circuits and Systems Letter

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From the Editor-in-Chief's Desk - Editorial

The **IEEE VLSI Circuits and Systems Letter (VCAL)** is affiliated with the **Technical Committee on VLSI (TCVLSI) under the IEEE Computer Societ**y. It aims to report recent advances in VLSI technology, education and opportunities and, consequently, grow the research and education activities in the area. The letter, **published quarterly** (from 2018), covers the design methodologies for advanced VLSI circuit and systems, including digital circuits and systems, hardware security, design for protection, analog and radio-frequency circuits, as well as mixed-signal circuits and systems. The emphasis of TCVLSI falls on integrating the design, secured computer-aided design, fabrication, application, and business aspects of VLSI while encompassing both hardware and software.

IEEE TCVLSI sponsors a number of premium conferences and workshops, including, but not limited to, ASAP, ASYNC,ISVLSI, IWLS, SLIP, and ARITH. Emerging research topics and state-of-the-art advances on VLSI circuits and systems are reported at these events on a regular basis. Best paper awards are selected at these conferences to promote the high quality research work each year. In addition to these research activities, TCVLSI also supports a variety of educational activities related to TCVLSI. Several student travel grants are sponsored by TCVLSI in the following meetings: ASAP2018, ISVLSI 2018, IWLS 2018, iSES 2018(formerly iNIS 2017) and SLIP 2018. Funds are provided to compensate student travels to these meetings as well as attract more student participation. The organizing committees of these meetings undertake the task of selecting right candidates for these awards.

The current issue of VCAL showcases the state-of-the-art developments covering several important areas: high speed VLSI interconnect, CMOS look-up table, SAR-ADC, Differential Amplifier etc. The peer-reviewed articles can be found in the section of "Features Articles". In the section of "Updates", upcoming conferences/workshops, call for papers and proposals, funding opportunities, job openings, conference report and Ph.D. fellowships are summarized. Additionally, a "Member News" section has been started from past issue onward covering the achievements of TCVLSI members.

We would like to express our great appreciation to all editorial board members (Yiyu Shi, Himanshu Thapliyal, Michael Hübner, Theocharis Theocharides, Jun Tao Shiyan Hu, Hideharu Amano, Mike Borowczak, Helen Li, Saket Srivastava, Yasuhiro Takahashi, Sergio Saponara, James Stine and Qi Zhu) for their dedicated effort and strong support in organizing this letter. The complete editorial board information is available at: https://www.computer.org/web/tcvlsi/editorial-board. We are thankful to our web chair Mike Borowczak, for his professional service to make the letter publicly available on the Internet. We wish to thank all authors who have contributed their professional articles to this issue. We hope that you will have an enjoyable moment when reading the letter! The call for contributions for the next issue is available at the end of this issue and we encourage you to submit articles, news, etc. to an associate editor covering that scope.

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Features

Frequency Improvement of 10-bit SAR-ADC using TSPC based Control Circuitry

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Abstract – SAR-ADCs are widely used today due to their low power dissipation at high resolutions. However, their frequency of operation poses as a challenging task. The presence of comparators, digital-to-analog converters (DAC) and control circuitries limit the speed of operation in SAR-ADC. This paper exploits means to fasten up the SAR-ADC operation using several control circuitries. Transmission gate CMOS, gate-diffusion based input and true single phase clocking based D flip flops are designed using generic process design kit 45 nm CMOS technology to design the control circuitry for comparison. The mean deviation, standard deviation of these are analysed using a set of Monte Carlo simulations with 1000 random trials. Post-layout simulations yield variation of delay and power to be 34 ps and 7.47 μW at a bit duration of 100 ps. The control circuitry is then further designed in a 10-bit SAR ADC which yields the frequency of operation of SAR-ADC to be lower for transmission gate based D flip flop, gate diffusion input based D flip flop and true single phase clocking (TSPC) respectively. The 10-bit SAR-ADC can function at a frequency of 2.3 GHz with TSPC based design.

1. Introduction

The advances in communication systems require very large bandwidth and high sampling rate conversion of analog-to-digital converters (ADCs) [1]. The higher sampling rate flash ADCs have design space requirements along with power dissipation. Several thermal noise falls in the spectrum and affects the signal parameters like signal-to-noise ratio (SNR) [2] and its related parameters when operating for higher sampling rate. These effects are getting worse in wireless communication device where ADCs act as an integral part of its functionality [3]-[4]. Several ADCs like flash ADCs, sigma-delta ADCs suffer from several drawbacks which include sparkle codes and oversampling that gives rise to complex circuits [3]-[5]. A solution to this is the use of successive-approximation-register ADC (SAR-ADC). Analog-to-digital conversion is carried out in several steps which limits the speed of operation and achieves speed of MS/s to GS/s.

Figure 1 depicts an SAR-ADC that requires `b' (resolution) periods for analog to digital conversion and one period for sampling of input signals. One single clock is used for functioning of the entire SAR-ADC. Clock generation outside the phase. In the sampling phase, the sample/hold (S/H) switch turns on and samples the input signal to the digital-to-analog converter (DAC) array. DAC array [6] converts the digital approximation value to the analog signal to compare with the input reference signal. Then the S/H switch turns off and the phase starts by detecting the polarity of sampled input using the control ciruitry at the start-of-conversion phase (SOC). The DAC array then converts this digital signal into analog signal which marks the end of the conversion phase [7]. The sampling-conversion-storage-sampling process is iterated till the entire shift register is updated. The SAR comparison architecture can be automatically triggered even in the absence of any clock architecture. DACs and the control circuitries present in the architecture also limit the performance of ADC.

2. Problems associated with SAR-ADC

Though the SAR-ADC is very economical as compared to other ADC architectures, achievement of high precision with acceptable rate is a challenging task. Key limitations and feasible solutions through the improvement of control is described as:

1. The conversion in SAR-ADC takes more time of around 1/2 least significant bit (LSB) with large number of bits resolution [8]. Control circuitry must function at a faster rate than that speed of operation.

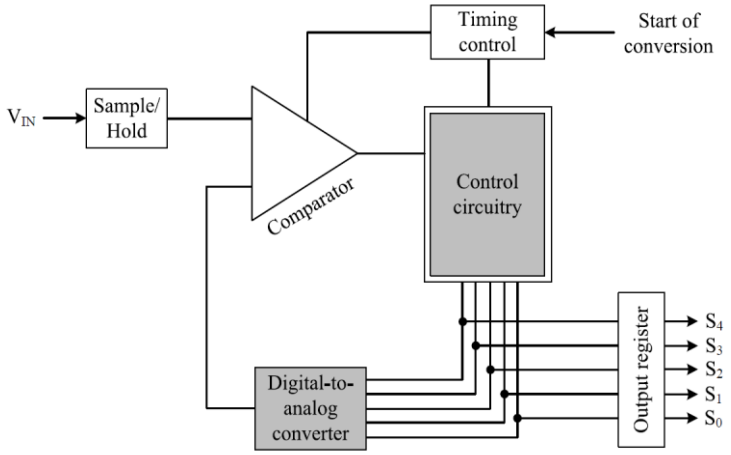

Figure 1: A typical topology of successive approximation register ADC

2. Energy dissipated due to the digital-to-analog converter (DAC) switching is also an issue in the design. Doubling of LSB relaxes the limit of noise and offset. A fast register based control circuitry can be used to aid the DAC switching for the charging and discharging of capacitors [9].
3. Now-a-days, the systems are designed using lower technology nodes to meet the needs of higher speed and design density. It fulfills the demand of reduction of voltage that gives rise to an augmented supply and Figure-of-Merit (FoM) [10] remains very low in the range of some hundreds for SAR-ADC. The higher operating frequency with lower power dissipation yields lower FoM which is very essential for SAR-ADC operation.

This paper presents a SAR ADC by optimizing the control circuitry. Section 2 provides a brief discussion on various control circuitries. The following sections describe topologies of D flip flop used for control circuitry design, their comparison and finally the conclusions are drawn in Section 5.

3. State of Art

Control circuitries comprise a basic unit of SAR-ADC design. This module is responsible for a continuous DAC switching for a full conversion. A set of shift registers, decoders and switching blocks are primary sub-modules involved. The role of digital circuits in power consumption is high owing upto 80 % of total power dissipation. Several advanced techniques are used like voltage down scaling technology and changes in design scenario to reduce this power. As externally driven clock generate high noises such as jitter and skew, clocks are generated internally. Control circuitries are of synchronous or asynchronous type [11]. In an asynchronous control circuitry, the input frequency is equal to the sampling frequency whereas in synchronous circuits it is equal to the sampling frequency X (N+2).

The dynamic comparator generates these asynchronous/synchronous signals and sends it to the digital controlled circuit. At each rising edge of the sequencer, when the output is high capacitor bank terminals are connected to V_{DD} else ground. The prime idea of control circuitry is to improve the space allocation. Asynchronous decoder based designs are used in some architectures which consume huge power to control the capacitive DAC network for switching the circuits as depicted in Figure 1. The control circuitry detects each bit decision from the comparator and locks it for next processing. The capacitive array needs to be discharged to a low voltage (V_{LOW}) after every conversion. Therefore, the control circuitry must function at half the frequency of the DAC. A decoder is used to provide clocks to the shift register in this regard which provides the next set of digital values to be converted. The shift register takes the comparator output after each conversion to detect the difference between the real input and converted output from DAC. Shift register outputs are fed to a selector bank for synchronization between DAC and control circuit. The outputs of the bank are used

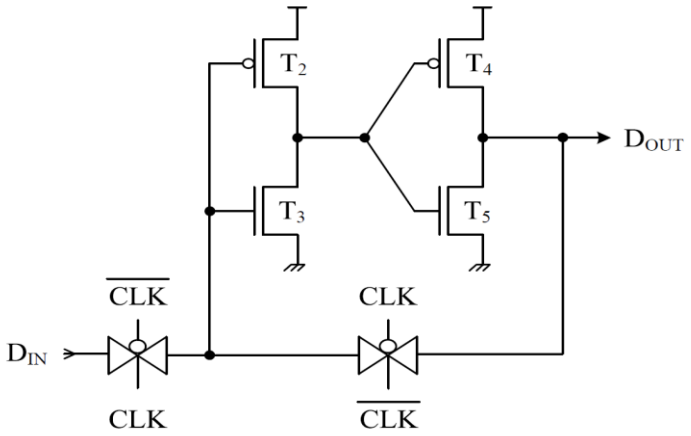

Figure 2: Transmission gate based D flip flop

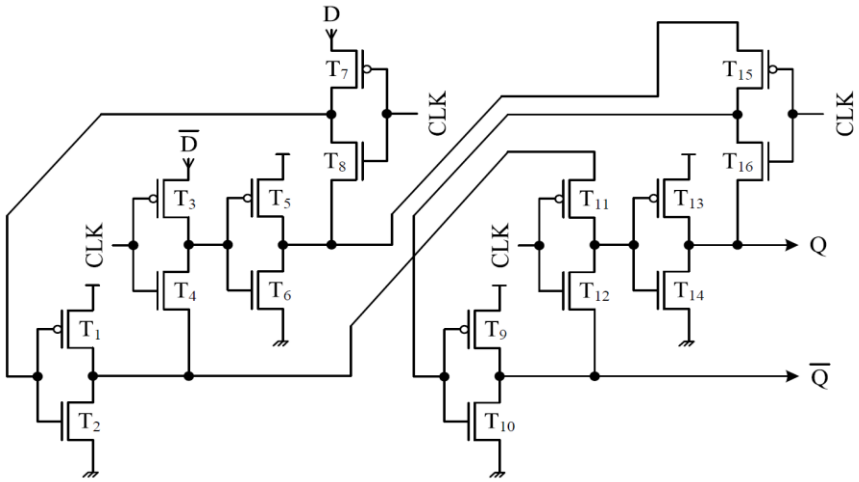

Figure 3: GDI based D flip flop

to provide the voltage levels to DAC. The iteration carries forward till all the 10-bit digital outputs are found. The operating frequency is severely affected by the frequency of these control circuits in SAR ADCs.

4. Shift Registers

D flip flop is primarily used for designing shift registers since it stands as a state holding element. Available D flip flops use one of the logic styles: Single Edge Trigger (SET), Double Edge Trigger (DET), Pass Transistor Logic (PTL), Adaptive Coupling (AC), Hybrid Latch Flip Flop (HLFF), Transmission Gate (TG) and Gate Diffusion Input (GDI). The mentioned techniques can form trade-off between delay, design space and power consumption. These D flip flops are designed using CMOS, clocked CMOS (CCMOS), GDI based MUX, power phase coding (PC) and true single phase clocking [12]-[15].

Static CMOS logic style to design D flip flop for shift registers comprises equal number of PMOS and NMOS transistors. The transmission gate based D flip flop shown in Figure 2 comprises two CMOS transmission gates and two inverters [12]. It is a level triggered flip flop. During the positive clock pulse, the input is sent to the output through a buffer. When clock is at its negative edge of flip flop then the previous output of is held by the latch and the input cannot change the state of the flip flop. Since the TG provides a lower ON state resistance, the latching becomes fast [13]. GDI based logic style for designing a D flip-flop is presented in [14], [15] which has three terminals: common gate of nMOS

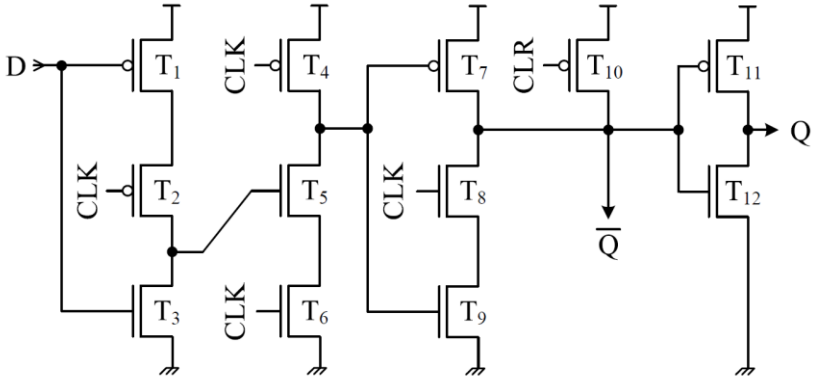

Figure 4: TSPC based D flip flop

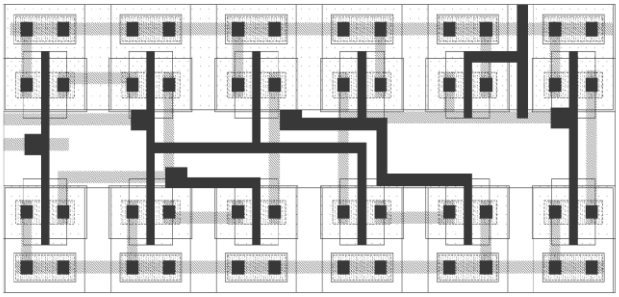

Figure 5: Extraction layout of TSPC based design

and pMOS (G); the one through drain or source of the pMOS (P); and an input via either drain or source of nMOS (N). The pMOS and nMOS bodies are connected to P and N respectively. Gates of these can be controlled through the CLK signal which create two alternate paths for HIGH and LOW. Figure 3 shows the master-slave GDI based D flip flop. The design comprises two units of D flip flop. First one is called master and second one is called slave. During the positive clock pulse, master follows the output. When clock is at its negative edge of flip flop then the slave comes into function, the master stops working. The previous output of the master is held by the slave and at that time there is no effect on master as it is in off state. The presence of this master-slave design eliminates the metastability of the design.

The change of state occurs for transmission gate based design whenever there tends to be an input transition for clock duration of small intervals. The reset time required is full one transition period. If instead of the entire transition period, half or three fourths of the reset period is used, then the time duration could be improved. There lies the attempt to improve the DAC performance which in turn improves the ADC speed. The reset phase of the D flip flop transition could be used for DAC switching.

True single phase clocking (TSPC)

The primary modification in the true single phase clock (TSPC) based design includes the working of the intermediate second and third stage in the precharge and hold mode. Addition of these stages creates a domino logic that can change the output while passing through the first inverter. The output stage can be reset directly without any change in the data input through CLR signal. This operation allows faster transition of the output. In contrast with the cascaded TSPC, the preceded third stage stores the value and an exact zero order hold is made possible. A TSPC logic based D flip flop is shown in Figure 4. At the negative level of the clock, first inverter is turned ON which allows the other inverter

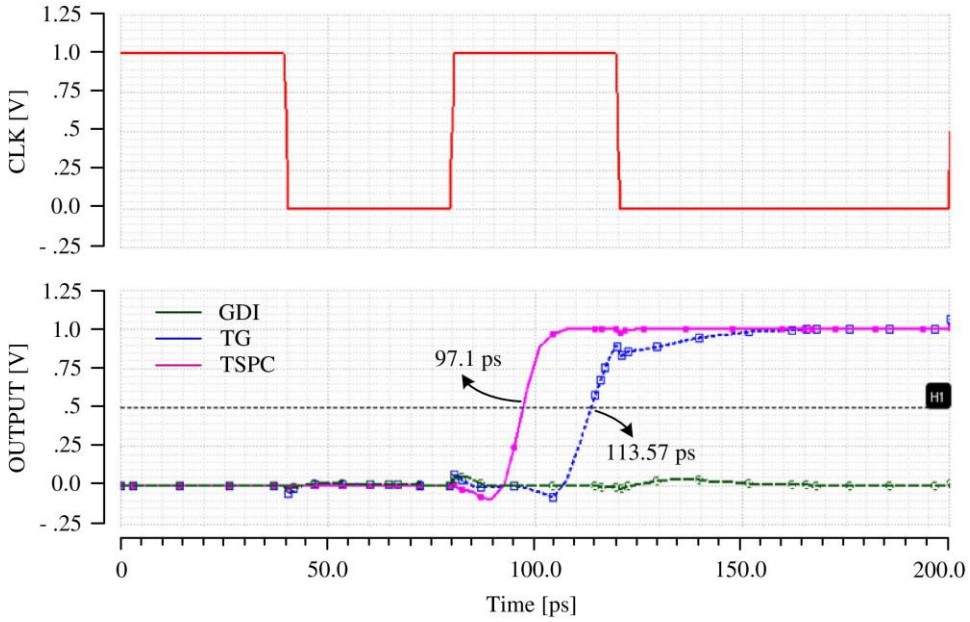

Figure 6: Timing diagram for all the compared D flip flop at a bit duration of 80 ps.

input to reach at transistor T5. The dynamic inverter is set at precharge phase since transistor T7 is turned OFF. The final inverter during this period can hold the value and output is remained stabilized when the clock is in low level. The high phase ensures that the earlier inverted input (D) is re-stored. During this period, the second inverter starts evaluation. Therefore, the D value loaded during the lower level can reach at output Q and remained until a high level of clock is reached. Certain advantages of TSPC based flip-flop over the TG design are:

- The TG based design has a feedback path at the output which increases the load capacitance at the output. The TSPC has no charge-sharing issue. Absence of load capacitance also increases the speed.
- An extra transistor T8 is added in the third stage. If this is LOW, then this stage does not behave like an Inverter. Rather the output is floated instead of making it an internal node. So, the design has a better robustness.
- Thirdly, if T8 is eliminated, then T7 and T9 will behave like a ratioed logic. The node cannot reach perfect high at times and there will be no full discharging path. Simulation result shows that the circuit is faster but at the cost of little extra dissipation. To keep a better power-delay product, it is chosen. However, the sizing of critical path can lower the delay which will in turn improve the operating speed.

5. Results and Discussions

The TSPC based SAR architecture is designed using 45-nm generic process design kit (GPDK) at a layout area of 4.781 $(mm)^2$ as shown in Figure 5. The simulations are carried out at a temperature of 27^oC and supply voltage of 1 V. All simulation designs have been carried out with the transistor size of W/L : 120/45-nm for a standard comparison. The results are plotted in Figure 6 with a bit duration of 80 ps. It is seen that GDI based D flip flop fails to function at a high frequency of 23 GHz, whereas TG based and TSPC based flip flop are functional at such a high frequency. It is seen that TG based design fails to set/reset during the time duration as shown in the Figure 6.TG and TSPC based design shows transition but with a delay. TG based design requires three fourths time of the clock duration for complete functioning. However, TSPC based design requires one fourth of the clock duration for transitional phase. In this way the speed of the architecture is improved to a large extent.

The TG based flip flop yields much delay of around 33 ps and TSPC based D flip flop yields delay of 17 ps and GDI based design fails to operate at 100 ps bit duration. TSPC based architecture is tested over variation for Monte Carlo (MC)

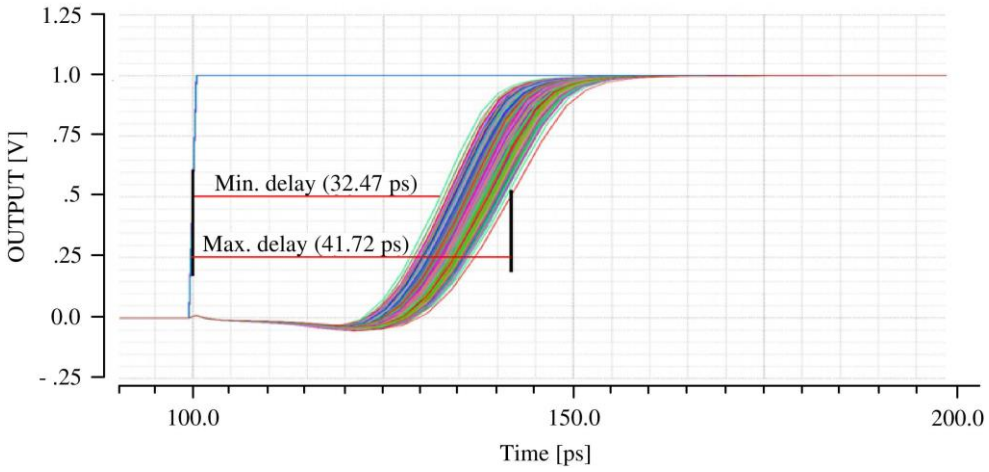

Figure 7: Simulation results of TSPC based design with 1000 Monte Carlo trials.

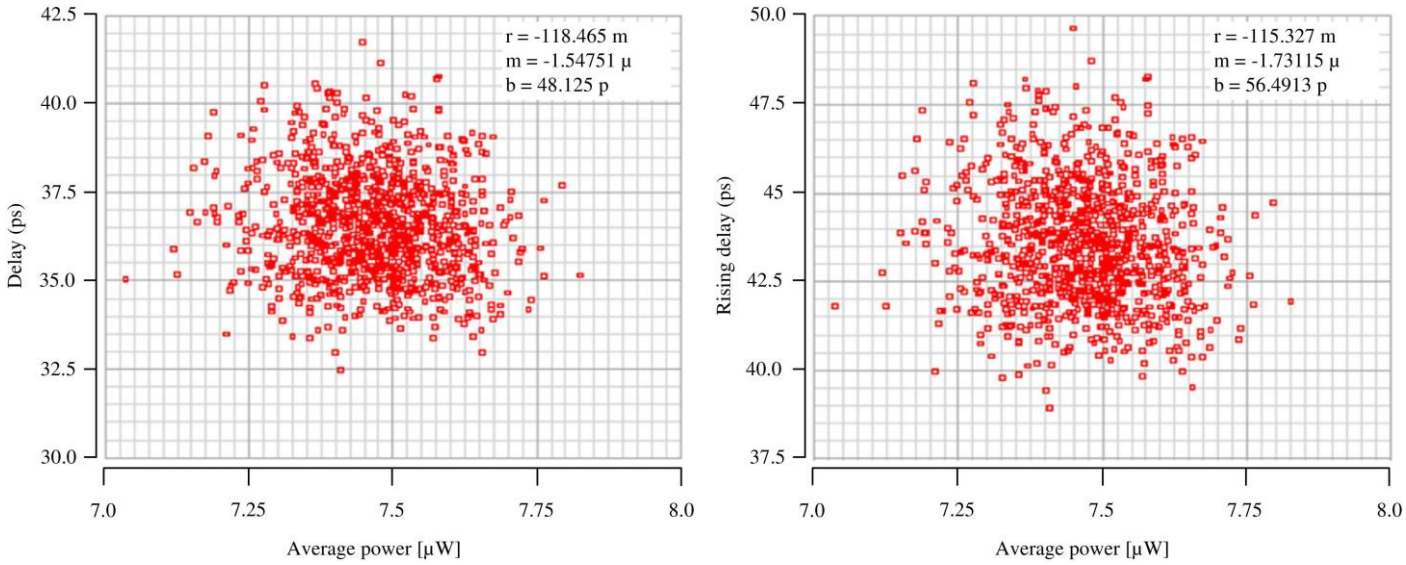

Figure 8: Scatter diagram plot for 1000 Monte Carlo trials.

trials of 1000 as presented in Figure 7.

The average power dissipation is 7.47 µW with delay of 34 ps. The delay is seen to be 54 ps for slow-slow (SS), 39 ps slow-fast (SF), 34 ps for fast-slow (FS), 26 ps for fast-fast (FF). The average power consumed is 6.64 µW, 7.61 µW, 7.18 µW, 8.49 µW with process variations of SS, SF, FS, FF respectively. Scatter diagram of the rising delay and average power are illustrated in Figure 8. It shows less scattered points in the delay as well as power metrics with moderate variation in the rising ML delay. A standard deviation of only 1.482 ps in the average delay as seen from Figure 9 with a lower mean value certainly proves the stability of the design. TSPC based D flip flop has been used for design of 10-bit SAR-ADC and it has been found that the ADC could function at around 2.3 GHz and therefore the operating frequency of SAR-ADC is seen to be improved compared to [1]-[7]. The ultra-wide band (UWB) transreceivers require high data date of operation. These could help in the design of such applications owing to its high data rate.

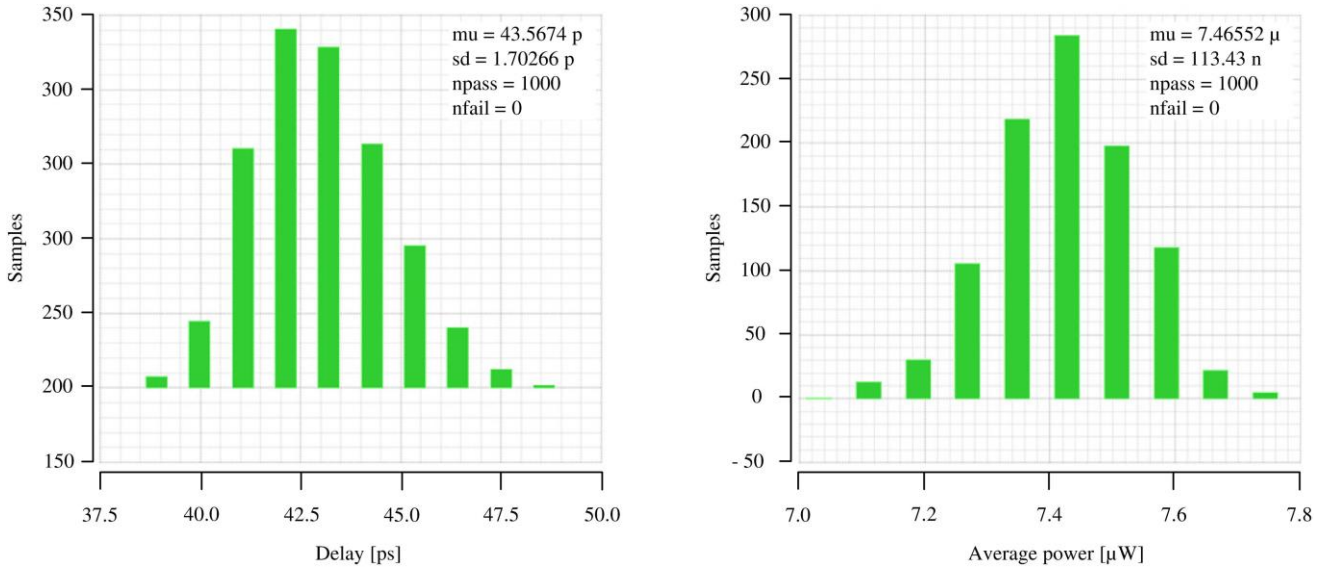

Figure 9: Histogram plot for 1000 Monte Carlo trials.

6. Conclusion

The TSPC based D flip flop functions well for high operating frequency and it could operate at 2.3 GHz for SAR-ADC. The TG based D flip flop though could function at a bit duration of 100 ps, however with a high delay necessitating higher reset margin and the GDI based D flip flop could not function at that frequency at all. All the comparisons have been carried out with default transistor sizing for effective comparison as the increase in transistor size leads to increase in power dissipation for a design. Effective transistor sizing would provide feasibility for further increasing the operating frequency of SAR-ADC. Thus, this paper exploits the design aspects in control circuits for SAR-ADC which further helps in improving the sampling frequency of SAR-ADC.

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Features

Accurate mid-band analysis of the differential-amplifier with active current-mirror load

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Abstract – This letter provides a new accurate mid-band analysis of the differential-to-single-ended converting differential amplifier with active current-mirror load. This small-signal analysis is also considerably simpler than previous methods that are available in CMOS textbooks and other published sources. Unlike previous methods the presented technique does not employ any Norton's/Thevenin's transformations nor does it require the determination of impedances using external test sources. The analysis shows that the actual mid-band gain of the differential amplifier with current-mirror load is only a fraction of the standard gain expression provided by textbooks and other articles. The presented analysis has not been reported before in open literature in any form.

1. Introduction

Differential amplifier with active current-mirror load is a basic building block in analog integrated circuits and analog signal processing. It is also often employed as a differential-to-single-ended converter in continuous-time and mixed signal analog VLSI circuits. A small-signal mid-band analysis of this fundamental analog building block is provided in the widely used popular textbook [1]. There are two solutions provided in [1] which employ complicated analysis technique requiring Norton's/Thevenin's transformations and/or the determination of impedances using external excitations. Also most classic texts [2, 3, 4, 5] do not provide any accurate and detailed small-signal analysis of the differential amplifier with current-mirror load. The authors in [3] provides an "intuitive" small-signal analysis using the current-mirror copy function without considering the current-mirror load which thus does not yield the accurate gain expression. In several recent articles [6, 7, 8] this author provided simplified small-signal analysis for a large number of various gain stages that were not available before. In this brief a new small-signal mid-band analysis of the differential-amplifier with current-mirror load is provided considering the current-mirror load which is simpler than [1] and more accurate than [3]. Standard symbols [1, 2, 4, 5] have been used here for describing all the MOSFET parameters in the small-signal mid-band analysis following the general convention in analog integrated circuit analysis. Also, appropriate DC, AC and composite voltage/current signal notations are employed. It is worthwhile to mention here that, all voltages and currents in lower-case alphabets along with upper-case subscripts are quantities containing both a large-signal DC bias (quiescent) value and a small-signal (AC) fluctuation (perturbation) superimposed on it. All voltages/currents in uppercase alphabets along with uppercase subscripts are DC bias quantities, and all voltages/currents in lowercase alphabets along with lowercase subscripts are AC perturbation quantities.

2. New simple and accurate analysis of the differential amplifier with active current-mirror

A differential amplifier with active current-mirror load is shown in Figure 1 along-with the composite input and output signals and DC bias voltages. Next, Figure 2 shows its AC equivalent circuit with all the bias voltages at AC ground. For a matched input differential-pair the drain of M3 (*d3*) can be considered to be at AC-ground so that the input differential-pair can be decomposed into two half-circuit components near the AC-ground. Figure 3 shows this decomposition of the input circuit for a matched input differential-pair. Here,

$$v_{\mathrm{d}} = (v_{\mathrm{in1}} - v_{\mathrm{in2}}) \qquad (1)$$

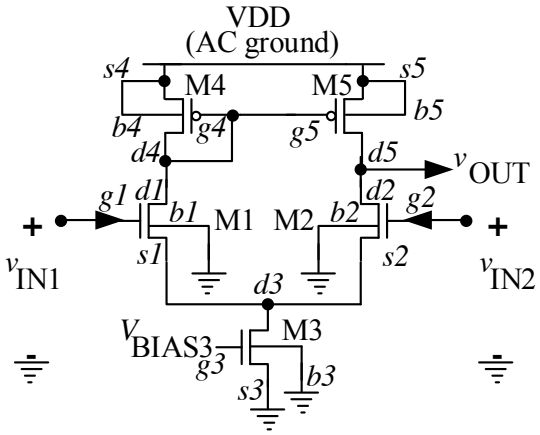

Figure 1: A differential amplifier with active current-mirror load.

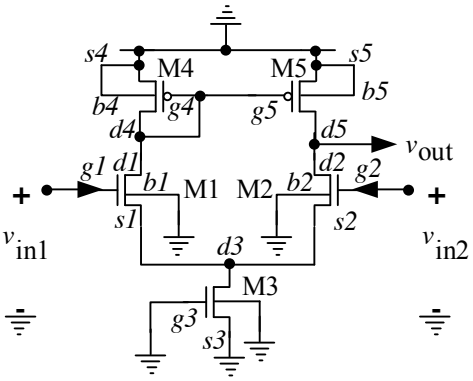

Figure 2: AC equivalent circuit of the differential amplifier with active current-mirror load.

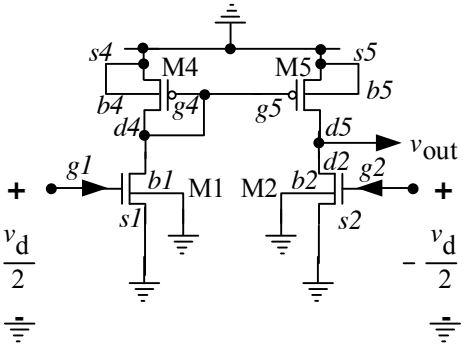

Figure 3: The decomposition of the input circuit of the differential amplifier with active current-mirror load for a matched input differential-pair.

Next, using the small-signal models, Figure 4 shows the complete small-signal equivalent circuit of the differential-pair with current-mirror load. Here the impedance of the diode-connected load (R_{M4}) is given by [6],

$$R_{M4} = \frac{1}{g_{m4.5} + \frac{1}{r_{o4,5}}} \qquad (2)$$

Where, $g_{m4.5}$ is the trans-conductance and $r_{o4,5}$ is the output impedance of the matched current-mirror pair (M4, M5). Since the transconductance current source of M1 is flowing out of the parallel combination of its output impedance and

the diode-load of the current-mirror pair, the small-signal voltage at the gate of the current-mirror pair (as well as the drains of M1 and M4) is given by,

$$v_{g4,5\_d1,4} = -g_{m1,2}\frac{v_d}{2}\frac{1}{g_{m4.5}+\frac{1}{r_{o4,5}}+\frac{1}{r_{o1,2}}} \quad (3)$$

Next, the current-source current of M5 can be expresses as,

$$g_{m4,5}v_{g4,5} = -g_{m1,2}\frac{v_d}{2}\frac{1}{g_{m4.5}+\frac{1}{r_{o4,5}}+\frac{1}{r_{o1,2}}}g_{m4,5} \quad (4)$$

which is shown in the reduced form of the equivalent circuit in Figure 5. The final form of the small-signal equivalent circuit for the decomposed differential-pair with active current-mirror load is shown in Figure 6. It consists of just a single current-source formed by the algebraic sum of the two in-phase current-sources along with a parallel combination of the output impedances of M5 and M2. The single current-source is given by,

$$i_{src} = -g_{m1,2}\frac{(v_{in1}-v_{in2})}{2}\left[\frac{1}{g_{m4.5}+\frac{1}{r_{o4,5}}+\frac{1}{r_{o1,2}}}g_{m4,5}+1\right] \quad (5)$$

The negative value of i_{src} signifies that the composite dependent current-source is now in-phase with the output current/voltage polarity. The final accurate differential-to-single-ended gain expression is thus given by,

$$A_v = \frac{g_{m1,2}\frac{(v_{in1}-v_{in2})}{2}\left[\frac{1}{g_{m4.5}+\frac{1}{r_{o4,5}}+\frac{1}{r_{o1,2}}}g_{m4,5}+1\right](r_{o1,2}//r_{o4,5})}{(v_{in1}-v_{in2})} \quad (6)$$

or,

$$A_v = g_{m1,2}\frac{1}{2}\left[\frac{1}{g_{m4.5}+\frac{1}{r_{o4,5}}+\frac{1}{r_{o1,2}}}g_{m4,5}+1\right](r_{o1,2}//r_{o4,5}) \quad (7)$$

which is different from the standard expression used in most textbooks and other published avenues, given by,

$$A_v = g_{m1,2}(r_{o1,2}//r_{o4,5}) \quad (8)$$

Eq. (8) is the same in magnitude to the small-signal mid-band gain of a fully-matched fully-differential amplifier with current-source load.

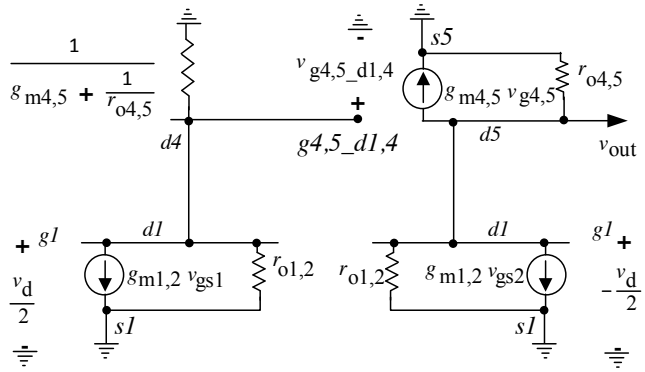

Figure 4: Small-signal equivalent circuit for the decomposed differential-pair with active current-mirror load.

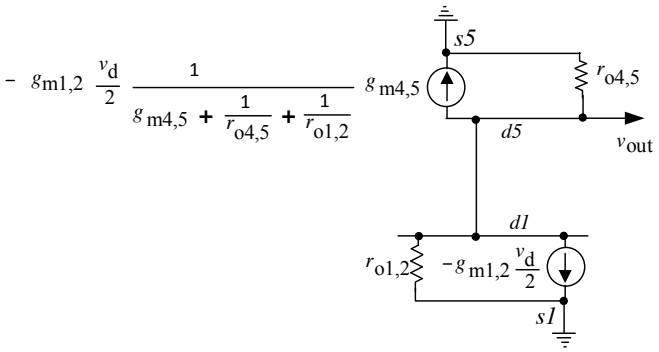

Figure 5: Reduced form of the small-signal equivalent circuit for the decomposed differential-pair with active current-mirror load.

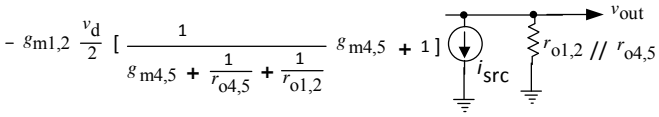

Figure 6: Final form of the small-signal equivalent circuit for the decomposed differential-pair with active current-mirror load.

Comparing (7) and (8) it is clear that the mid-band gain expression (mid-band gain magnitude) of a fully-matched differential amplifier with matched current-mirror load is not the same as that of a fully-matched fully-differential amplifier with current-source load. The new eq. (7) incorporates the effect of the current-mirror load as distinct from the current-source load. Eq. (8) is valid only for very large output impedances of the differential-pair and current-mirror-pair devices which may not be valid for today's nano-metric analog CMOS circuits [9]. Taking the ratio of (7) with respect to (8) the mid-band gain-ratio has the form,

$$G_{ratio}=\frac{1}{2}\left[\frac{1}{1+\frac{\sqrt{I}}{\sqrt{2\mu_p C_{ox\_4,5}\frac{W_{4,5}}{L_{4,5}}}}[\lambda_{4,5}+\lambda_{1,2}]}+1\right] \qquad (9)$$

Where, I is the DC bias-current in each side of the differential-pair and λ is the channel-length modulation parameter. With λ being inversely proportional to the channel-length, considering today's deep nano-metric processes [9], the actual mid-band gain is only a fraction of the standard mid-band gain as expressed by (9). The standard (conventional) expression in (8) is only valid for very long channel length for which (9) approaches unity.

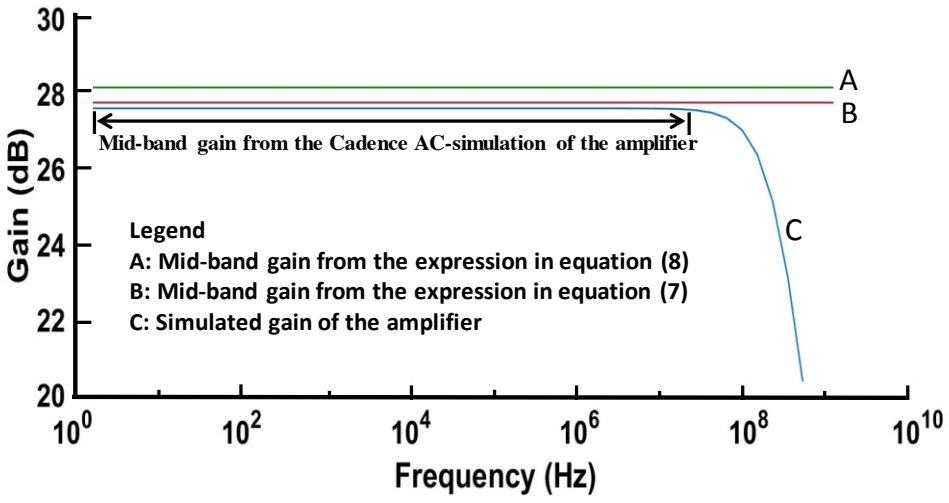

Figure 7: Comparison of the Cadence Spectre simulated mid-band gain with the calculated mid-band gains using the expressions in the new eq. (7) and the conventional eq. (8).

3. Numerical results

In order to demonstrate the accuracy of the mid-band gain expression in (7) compared to the conventional expression in (8), a design example of differential amplifier with current-mirror load in Figure 1 was simulated on Cadence Spectre circuit simulation tool. The Global-Foundries 130 nm 8HP process technology PDK (process design kit) was employed for this circuit simulation. For DC-bias setup the designed circuit used a supply voltage of 1.5V and a half-circuit drain-current of 64.08 μA with a total DC-bias current of 128.16 μA. The device sizes (W/L ratios) were as follows, for M1 and M2 $W_{1,2}/L_{1,2}$ = 19.6μm/0.3μm with the threshold-voltage (V_{th}) = 347.1 mV, for M4 and M5 $W_{4,5}/L_{4,5}$ = 12μm/0.3μm with the threshold-voltage (V_{th}) = -285.9 mV, and for M3 W_3/L_3 = 24μm/0.3μm with the threshold-voltage (V_{th}) = 309 mV. Figure 7 depicts the comparison of the MATLAB calculated mid-band gains along-with the graph of the Cadence AC analysis gain for this design example. The calculated gain using (7) and (8) were respectively 24.38 (27.74 dB) and 25.54 (28.14 dB), while the Cadence simulated mid-band gain was 23.96 (27.59 dB) as shown in the Figure 7. The results thus clearly indicate that the expression in (7) is more accurate than the expression in (8) being closer to the simulated mid-band gain obtained through Cadence circuit simulation. This is because (7) includes the effect of the current-mirror load for all values of device output impedances, whereas (8) provides the ideal-case mid-band gain for very high device output impedances.

4. Conclusion

A simple and accurate small-signal mid-band gain expression for the differential amplifier with current-mirror load has been derived. The expression indicates that the actual gain which includes the effect of the current-mirror load is only a fraction of the gain expression provided in textbooks and other open literature. This new expression provides a more accurate gain for today's deep nano-metric CMOS VLSI processes.

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Features

Investigation of single wall/multi wall carbon nanotube composites with bending effect for the application of high speed VLSI interconnect

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Abstract – The paper presents analysis of Delay crosstalk and effect of bending on Delay by using high frequency equivalent single conductor circuit model (ESCCM) of single wall and multi wall carbon nanotube (SWCNT, MWCNT). A mixed SWCNTs and MWCNTs of different figurations are discussed to get better performances. To make the proposed model more realistic, bending effects on six different CNT arrangements are considered. The distributed circuit components were evaluated for both simple and bended structure models of proposed interconnects. Dynamic cross talk performances with propagation delay are investigated using mixed carbon nanotube bundles and ESCCM model. Proposed mixed CNT configuration named as Mix-IV shows better delay performance among six different models. Two different switching arrangements, like as in-phase and out-of-phase are shown for cross talk delay measurement.

1. Introduction

In the Nano scale device application region, Carbon Nano Tubes (CNTs) are most prominent and attractive materials for high current capacity, long mean free path, unique electrical, mechanical and thermal properties [1-6]. Increase of resistance of metal interconnects (Cu) is due to the high frequency and reduced mean free path. High frequency is related to the issue of reliability and RC delay effect [7-9]. On the other hand, heat production due to Joule heating is also an important concern [7]. To get the balanced scaling factor and mean free path current density grows rapidly. So, for the high speed (DC level to 100GHz) application CNT may be the best replacement over metal interconnect [10]. As reported by the International Roadmap for Semiconductors, the interconnect problem is the major concern in the VLSI technology [11]. Based on the concentrically rolled up graphene sheets CNT is characterized as Single wall CNT (SWCNT) and Multi wall CNT (MWCNT). Different researchers are working (through modelling and simulation) on the crosstalk and propagation delay performances of SWCNTs and MWCNTs [12-14]. Different combinations like as only single wall CNT bundle, multi wall CNT bundle, single and multiwall mix bundle and CNT with metal mix bundle were investigated for getting the better delay and cross talk performances [15, 16]. To get the desired densely packed CNT bundles different diameter (on single and multiwall CNT) and distribution are undertaken for the high speed implementation [17-20]. Analytical model of the mixed CNT bundle (MCB) was proposed by Manoj et al. with different arrangement [15]. In the recent trend nano-technology and advance semiconductor architecture is also very much useful for different semiconductor device (along with VLSI) application [21-28].

In view of above discussion the content of this paper is organized as below. Six different mixed arrangements of single wall and multi wall CNT modelling phenomenon is discussed in the Section II. The bending effect of mixed-CNT bundles are investigated with different bending angle in the Section III. Impact on the crosstalk and delay performances of six different arrangements of SWCNTs and MWCNTs and bending effect are discussed in the Section IV and Section V.

2. Equivalent single conductor (esc) model of mix SWCNT and MWCNT

It is difficult to simulate circuit model of a bunch of channels of Mixed CNT Bundle altogether. To make it simple equivalent single conductor model is employed as shown in Figure 3. Single wall carbon nanotubes (SWCNTs) and multi wall carbon nanotubes (MWCNTs) with mix configurations are considered for the simulation models. Six different arrangements of SWCNTs/ MWCNTs are shown in Figure 1. Mixture of different bundles are named as (a) Mix-I, (b) Mix-II, (c) Mix-III, (d) Mix-IV, (e) Mix-V, (f) Mix-VI respectively. To compare the reported results of Manoj et al. [15] the height of the bundle and with of the bundle are considered as 168nm and 70nm respectively. Also, different global

lengths of interconnect transmission line are chosen as 100µm, 500 µm and 1000 µm accordingly. Numbers of CNTs for the proposed six different mixtures with ground facing SWCNTs and MWCNTs are mentioned in Table 1.

TABLE I
DIFFERENT MIXING ARRANGEMENTS FOR THE SIX DIFFERENT BUNDLES

Mixtures	No of SWCNTs and MWCNTs		No. of CNTs facing Ground	
	SWCNT	MWCNT	SWCNT	MWCNT
Mix-I	6500	45	51	02
Mix-II	271	208	02	10
Mix-III	4159	27	59	01
Mix-IV	226	210	01	115
Mix-V	1139	187	67	0
Mix-VI	1139	187	0	11

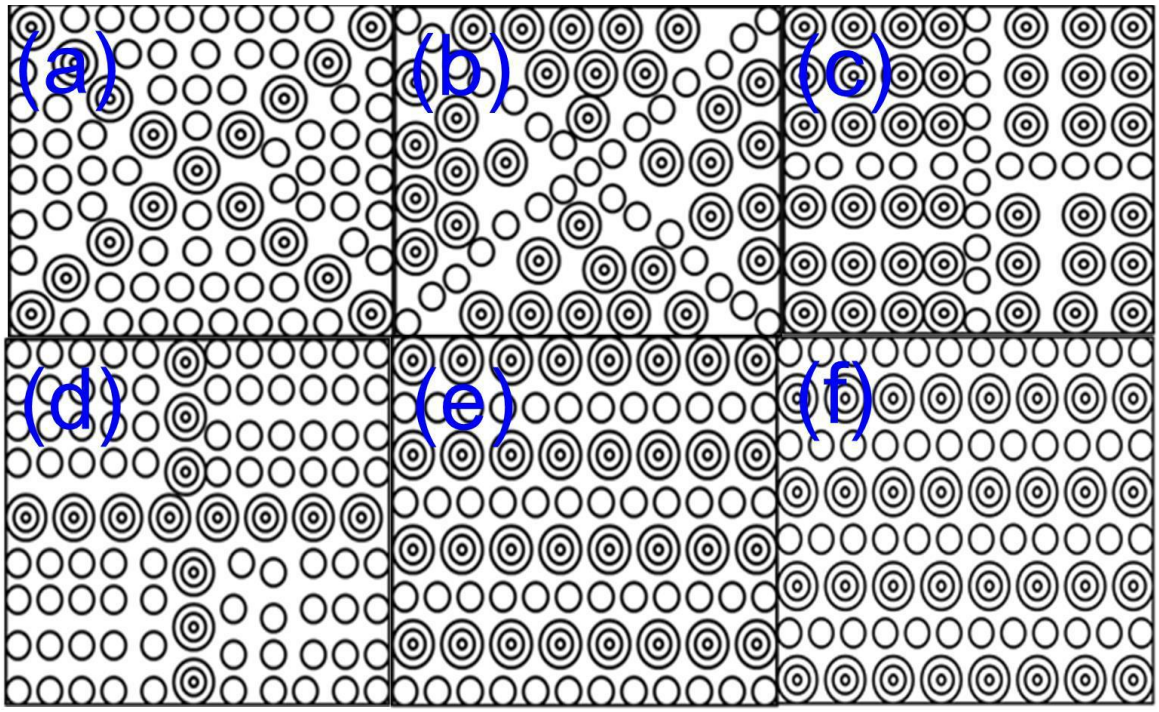

Figure 1: Schematic representation of proposed mixed SWCMT/MWCNT interconnects bungles with different orientations: (a) Mix-I, (b) Mix-II, (c) Mix-III, (d) Mix-IV, (e) Mix-V, (f) Mix-VI.

3. Bending model of SWCNT and MWCNT

The equivalent single conductor model for bended CNT configuration is shown in Figure 6. Four different bending angles ($\alpha=30^{o}$, $\alpha=60^{o}$, $\alpha=90^{o}$, and $\alpha=120^{o}$) were considered to investigate the bending effect on the coupling capacitance and bending delay. Schematic representation of the proposed bending arrangement with 500µm length and bending angle of $\alpha=90^{o}$ is shown in Figure 2.

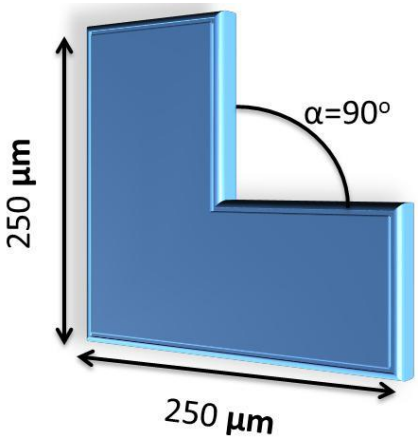

Figure 2: Schematic of proposed bending arrangement with 500 µm length and bending angle of α=90^{o}.

4. Performances of proposed model with validation

The ESC model with input/output configuration for the proposed six different SWCNT and MWCNT mix configuration is shown in Figure 3. Equivalent single conductance inductance and capacitance values are calculated from the equation (1) and (2) [15, 29, and 30].

$$L'_{esc} = L'_{kesc} + L'_{Eesc} \quad (1)$$

$$C'_{esc} = \left(C'^{-1}_{qesc} + C'^{-1}_{Eesc}\right)^{-1} \quad (2)$$

Where L'_{kesc}, C'_{qesc}, C'_{Eesc} and L'_{Eesc} are kinetic inductance , quantum capacitance, electrostatic capacitance and inductance due to the Bundle CNTs facing ground respectively. To measure the equivalent single conductor model resistances equation (3A) and (3B) is used.

$$R_{Desc} = \frac{R_0}{N_t} + R_p \quad (3A)$$

$$R'_{esc} = \left(\frac{h}{4e^2}\right)\frac{1}{\lambda_{mp} N_t}\ ;\ \lambda_{mp} = \frac{10^3 D_i}{(T/T_0) - 2}\ ;\ T_0 = 100\text{K} \quad (3B)$$

Where in equation (3A) R_0 , R_p and N_t are the DC resistance of CNT, metal nanotube contact resistance, and total number of conducting channels respectively and in equation (3B) h , e , λ_{mp} , D_i , T are plank's constant, electronic charge, mean free path of carrier, diameter of i_{th} shell of CNT and operating temperature respectively ([15] of manoj et al.]) The comparison results of the capacitance, inductance and resistance values of the six proposed models with existing MCB-VI [15] model are shown in Table II.

TABLE II
COMPARISON RESULTS OF SIX PROPOSED MODELS WITH MCB-VI

Interconnect parasitic	MIX-I	MIX-II	MIX-III	MIX-IV	MIX-V	MIX-VI	MCB-VI [15]
L'_{esc} (pH/µm)	1.7507	0.03602	2.7505	6.2901	4.5604	4.5688	36.49
C'_{esc} (pF/µm)	1600	114.26	1798	49.10	1993	466.90	62.83
R_{Desc} (kΩ)	3.5014	3.5050	3.5022	3.5050	3.5036	3.5036	3.50
R'_{esc} (Ω/µm)	1.11	0.895	1.75	0.89	0.91	0.91	0.79

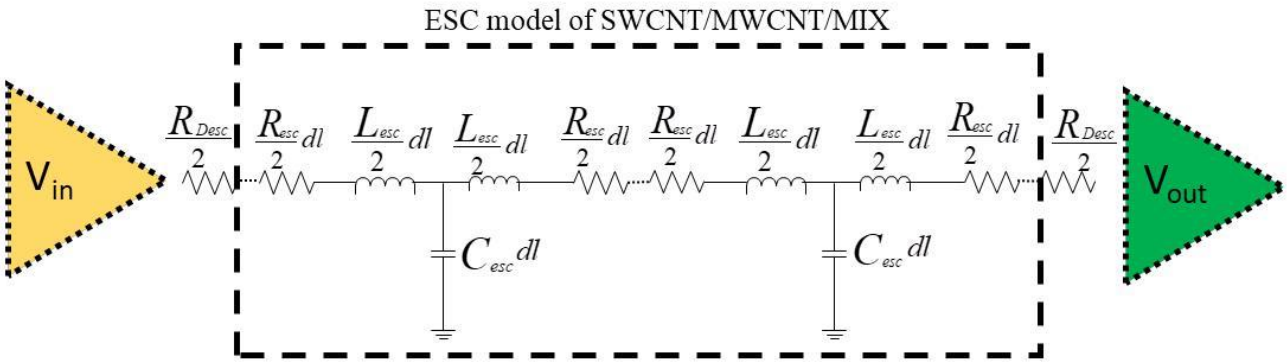

Figure 3: Equivalent single conductor circuit model (ESCCM) for the proposed interconnect structure

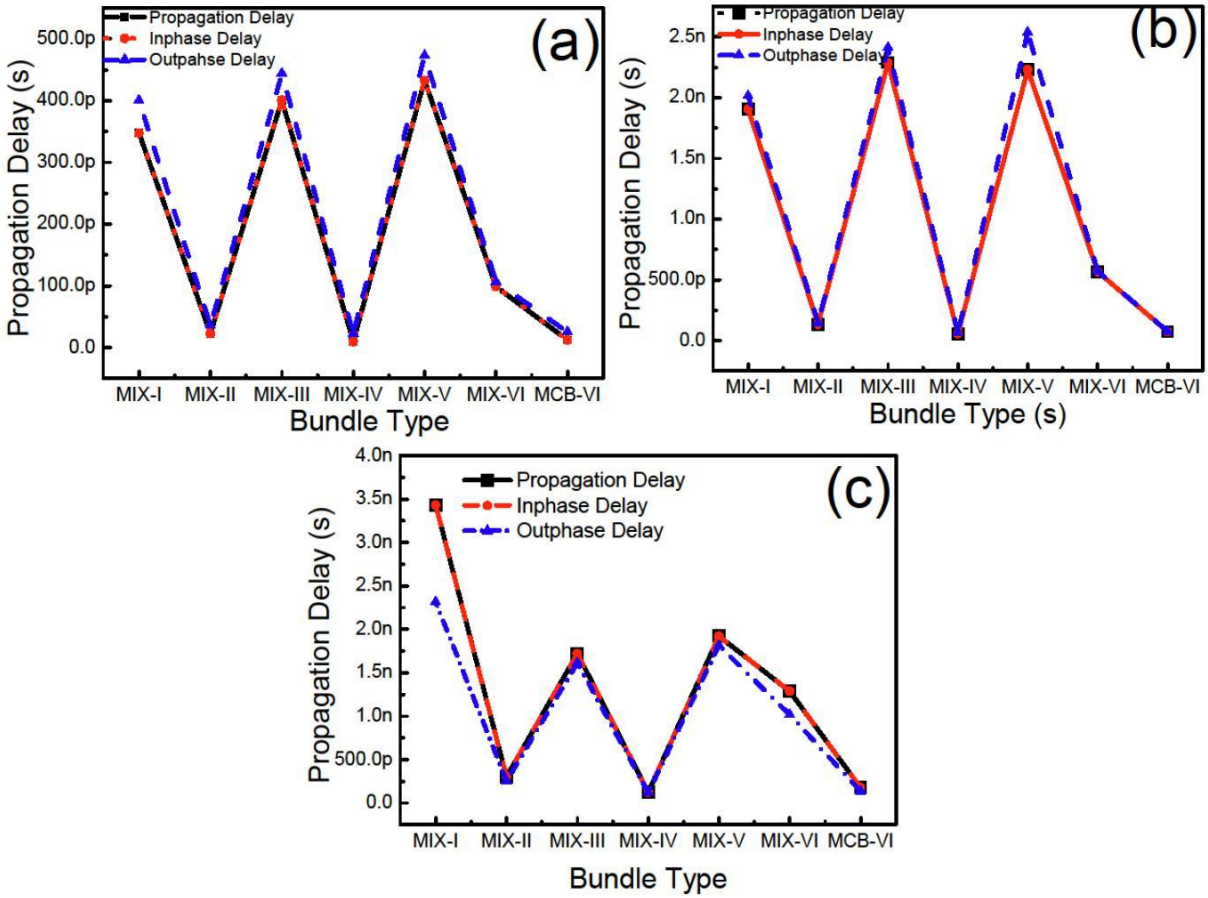

Figure 4: Delay measurements with and without cross talk phenomenon for the six different arrangements: (a) bundle length 100 µm, (b) bundle length 500 µm(c) bundle length 1000 µm.

The delay phenomenon in interconnect is occurring due to the large inductance and capacitance value. Figure 4 shows a delay measurement with and without cross talk phenomenon for the six different arrangements where (a) bundle length is 100 µm, (b) bundle length is 500 µm(c) bundle length is 1000 µm. Mix-IV shows better performance over all proposed arrangements and MCB-VI due low inductance and capacitance value (as mentioned in Table II). Percentage delays in cross talk delay measurement are shown in Figure 5. The reduction of delay in Mix-IV over other arrangement and MCB-VI is due to the better conductance at the centre of the mix CNT bundle and better shielding from the neighbouring CNT bundles [31]. It is seen in figure 5 that after Mix-IV the MCB-VI and Mix-II shows exhibits better performance. Circuit Simulation – Cadence spectre is used to simulate the delay performances.

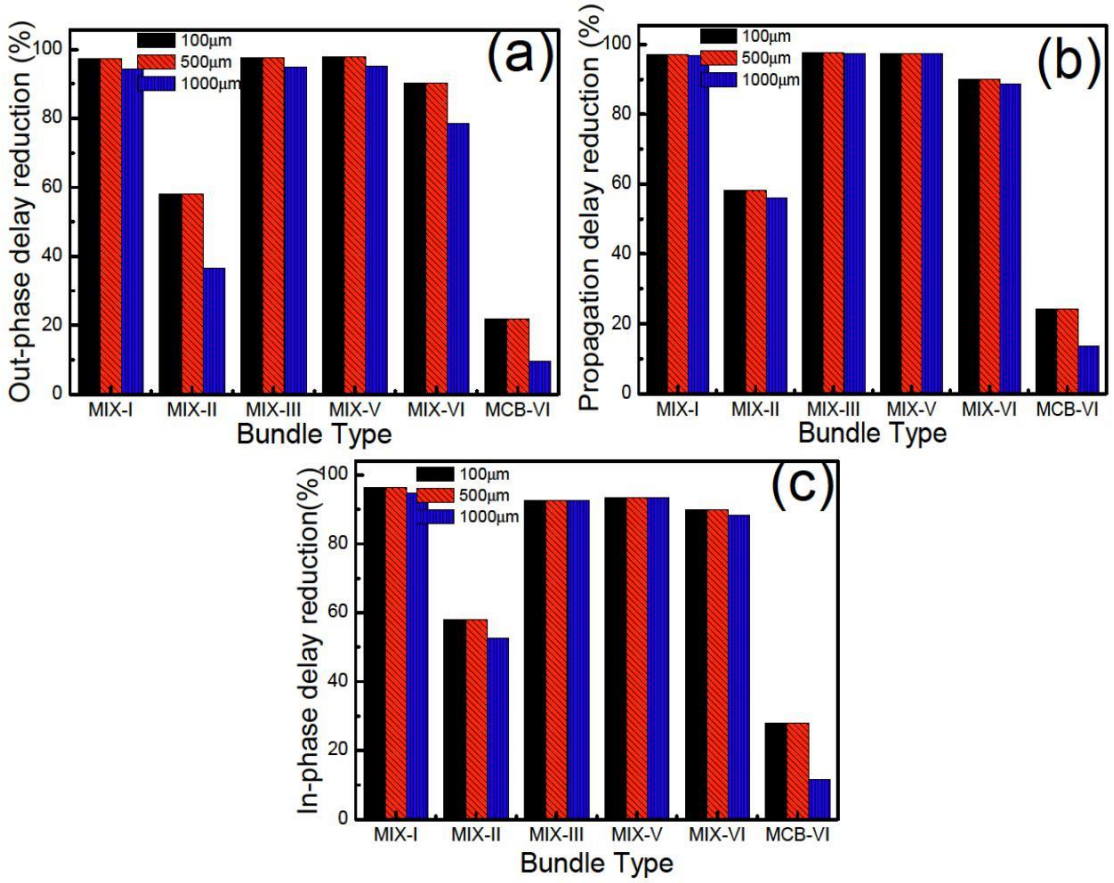

Figure 5: Percentage delays in cross talk delay measurement for Mix-IV in comparison with all proposed model and MCB-VI [15]: (a) Out-phase delay, (b) Propagation delay, and (c) In-phase delay.

5. Bending impact on crosstalk and delay performances

In this proposed model the effect of bending being is incorporated. Distributed coupling capacitance (C_{cm}) is added in the proposed equivalent single conductor circuit model (as shown in Figure 6).

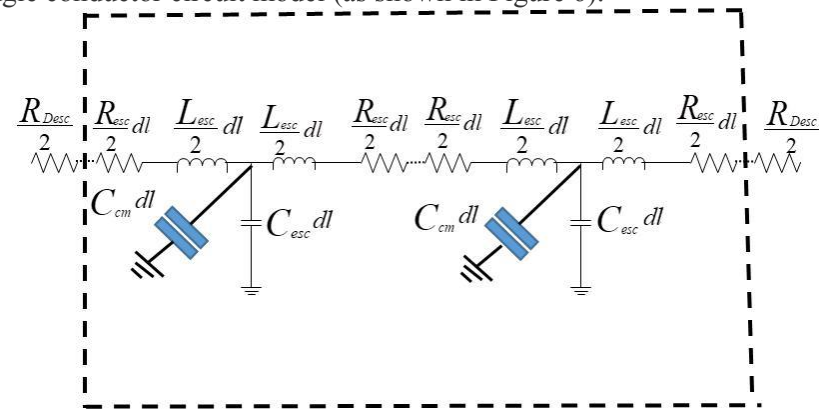

Figure 6: Equivalent single conductor circuit model for the bending configuration of different mix bundles.

It is seen in Table III that for the four different bending angles ($\alpha=30^o$, 60^o, 90^o, and 120^o) the coupling capacitance values are different. The capacitance value increases with increasing angle and the increasing length of the mixed bundle structure. This may be due to the increase of coupling capacitance value to the increasing coupling area. Figure 7 represents the delay performance for different mixing arrangements with the bending angle of $\alpha=90^o$. It is also seen in Figure 7 that the bending increases more delay in the equivalent single conductor circuit for the increased inductance and capacitance value.

TABLE III

CHANGE OF COUPLING CAPACITANCE VALUE WITH DIFFERENT BENDING ANGLE

Bending angle (α)	Length (μm)	Coupling capacitance (C_{cm}), F
α=30°	100 μm	7.3618x10^{-8}
	500 μm	1.6037 x10^{-6}
	1000 μm	6.0806 x10^{-6}
α=60°	100 μm	7.1702 x10^{-8}
	500 μm	1.5667 x10^{-6}
	1000 μm	5.9472 x10^{-6}
α=90°	100 μm	7.2403 x10^{-8}
	500 μm	1.5803 x10^{-6}
	1000 μm	5.9962 x10^{-6}
α=120°	100 μm	7.6609 x10^{-8}
	500 μm	1.6608 x10^{-6}
	1000 μm	6.26858 x10^{-6}

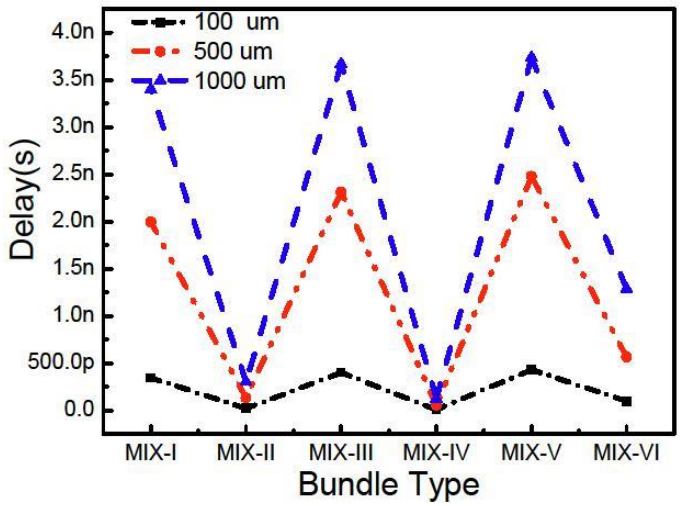

Figure 7: The delay performance for different mixing arrangements with the bending angle of α=90°

6. Conclusion

The work shows the practicability of the mix bundle CNT based interconnect for the higher speed applications. Six different mixing arrangements of SWNTs and MWNTs are considered for the simulation study. Among all, Mix-IV shows better performances (<100ps) for less equivalent single conductance inductance and capacitance values (6.2901 pH/μm, 49.10 pf/μm). Based on the circuit model, the propagation delays are captured with and without having of crosstalk for different bundle of arrangements. The effect of bending is considered with proper modeling. It is seen that the delay increases with increasing the bending angle (due to increase of capacitance values, 5.9472 x10^{-6} F for 1000 μm lengths and 60° bending angle). So the proposed model is very much effective the future study of temperature dependent study of interconnect.

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Features

Reliability Analysis & Performance of 3 input CMOS Look Up Table (LUT) in Various Nano Technologies

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Abstract – In this paper, the degradation in n-channel and p-channel MOSFETs are evaluated correspondingly. Negative Bias Temperature Instability (NBTI) and Positive Bias Temperature Instability (PBTI) are illustrated using different classification methods. Gate-diode or direct current IV is used to estimate trap generation (TG) during BTI. BTI tests are performed by DC Stress with different pressure biases and Temperature (T) values with discrete pulse duty cycle (PDC). The determined TG can show the remarkable similarity between NBTI and PBTI stress in DC pressure. Here, we examine the aging of transistor due to NBTI, PBTI & HCI (Hot Carrier Injection) of 3-input complementary look-up tables (CLUTs) by performing diverse executions over enlisted cadence simulations. Delayed degradation due to transistor aging differs on the alignment configure, the convention (input signal probability) as well as the peculiar CLUT implementation. Furthermore, CLUT has a substantial impact on the delayed configuration of the existing format used in the represented configuration LUT. Accurate aging and reliability analysis are crucial in considering these effects in the design cycle. Moreover, we figured out the leakage current, voltage, noise margin and power of designed CLUT. By this research methodological results, we proposed that our techniques can enhance the lifespan of LUT as well as FPGA in different nanoscale ranges of 90nm-45nm-22nm-11nm technologies. This detailed analysis has been done using Cadence Virtuoso tool.

Keywords- Reliability, PBTI, NBTI, HCI, Aging, 3 input CLUT, Nano Scale.

1. Introduction

Downscaling the CMOS technology, identical to the principal vitality of Moore's law, goes ahead with the necessary prerequisite for greater functionality, low power, long life and VLSI circuits more integration [1]. When this deterioration extends the size of the nano, several challenges abruptly propagate and precise themselves as physical impediments. Field Programmable Gate Array (FPGA's) forms the phenomenal and sustainable of the possible extent CMOS technology intersections due to their elevated capacity, reliability and sequential stipulations of sharp performance, low power digital and mixed-signal applications [20]. In FPGAs, lookup tables (LUTs) are the primitive blocks that map the Boolean functions. A0073 device is diminished due to technical scaling, this crisis has also found reliability concerns. These disputes include specific product variances, sub-leakage, power dissipation, increased circuit noise sensitivity and permanent (eg transistor aging) failures [16], [3]. Although FPGA has been successful in convalescing depletion performance and overall power consumption [10], [4], it has many reliability issues. Transistor aging is an imperative reliability challenges in nano-level CMOS technology. The provoking of aging will be recapitulated by the decrease of overall operation, the timing failure & the chip lifetime significantly [19].

Until recently, three significant causes were essential in aging research: Negative Bias Temperature Instability (NBTI), Positive Bias Temperature Instability (PBTI) & Hot Carrier Injection (HCI) [7], [8]. Although BTI's effect in previous technology was very low, it focused on reliability problem after the formation of high-k / metal gates [14], [20]. Although, the high κ Gate dielectric and metal gates transistors were earlier introduced, the effect of positive bias temperature instability (PBTI) enhances equal to NBTI & PBTI shown predominant appeal [13] [10]. Generally, NBTI and its equivalent PBTI, along with HCI, cause the transistor's initial voltage size to increase, and reduced mobility of carriers (NBTI effects PMOS transistors and PBTI will affect NOS transistors). Hence, exploring the effects of aging in these essential blocks helps to understand the behavior of the circuit under transistor aging. There is a greater possibility of direct effect of signal on NBTI -induced aging [13]. In order to diminish degradation, [8] the authors proposed to change the LUTs on a hierarchical basis for transistors to mitigate NBTI effect. In a study that was introduced, exposing FPGA chips to stress

conditions and reporting of aging, leakage current, voltage, power and noise margin. We implemented and verified the signified system techniques using academic tool cadence [14].
The frame of the paper is systematized as follows. Section II depicts NBTI & PBTI phenomena in more detail. Section III depicts HCI phenomena in more detail. Section IV illustrates the parameters methodology. Section V explains the literature reviews. Section VI explains the design of three input CLUT implementation. Section VII depicts the results evaluated for reliability aging and leakage parameters. Section VIII concludes the paper.

2. Aging model's effect on MOSFET

Aging is retiring of the terrible significant reliability dispenses in the nanometer regime. Circuit aging progressively intensifies the initial voltage of transistors and steadily ensues in degradation of the gate delay [18]. Ultimately, once the circuit delay surpasses time restraints, then the circuit flops. The age of transistors is precise to NBTI, PBTI, and HCI. NBTI, PMOS transistors desire pretend and PBTI, NMOS transistors will be pretended. Dualistic occurrences improve the transistor's voltage phase [12]. The HCI transpires as a rise of the transition in the source-gate of the transistor origin and the initial voltage escalation. This can intensely mitigate the VLSI chips functionality [10]. The aging aspects and their prototypes are illustrated in more specified manner as shown below. BTI has two different exposures.

A. Negative Bias Temperature Instability (NBTI)

NBTI is a prominent aging apparatus that directs to an initial voltage intensification when the Vgs for negative gate-source voltage to PMOS transistor to the gate is applied [8]. It hastens with an intensified in temperature. NBTI exposes an ascend in the drain current and trans-condensation of a MOSFET. While NBTI functioning with a negative gate to the source voltage, it pretends the devices that effect on P channel [9] [14]. While the fabrication, the hydrogen passivation is made considering the oxidation process to confiscate the Si molecules from the drooping. These feeble Si-H bonds can certainly break at the stress phase at higher temperatures, and this can lead to the generation of donors, such as the so-called Interfacial Traps, which is contended to be the major initiatives of the threshold voltage over time of the device. The H neutral atom has a slow distinction, while the H-H molecules form the H_2 molecule, which varies rapidly in the oxide that the H atom. Therefore, NBTI is the calculation of an continual trap generation at the Si/SiO_2 interface of the PMOS transistor [20]. During the NBTI pressure, the amount of interface traps is identical to the positive charges in the oxide group [12] [15]. PMOS exhibits the NBTI mechanism in the transistor, where it is clear that diffusing species of the H atom or the H2 atoms.

$$Si_3 \equiv SiH + H^+ \leftrightarrow Si_3 \equiv Si + H_2 \quad (1)$$

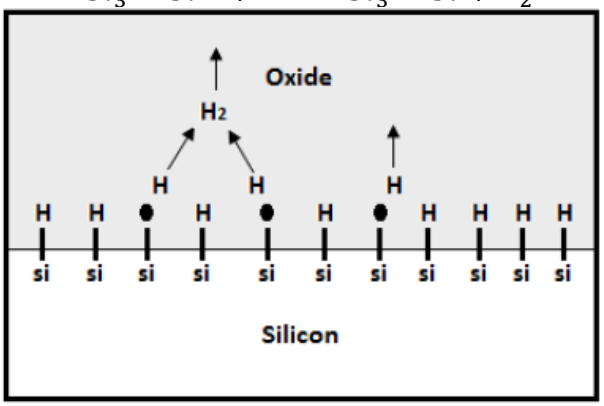

Figure 1: Tapes generation in Silicon (Si) & diffusion of Hydrogen (H2)

B. Positive Bias Temperature Instability (PBTI)

PBTI is additionally a reliability crisis in large-scale CMOS technologies. It implies to NMOS transistors. It is a major aspect in prohibitive k-dielectric and metal-powered technology [6]. The BTI feed and the dielectric interface are the results of the trap generation. BTI has two assorted treads (see Figure 1). In this paper, the various nano-meter technologies evaluated that NMOS has Vgs = 0.7 (threshold voltage) Vds = 0 are measured under the pressure of the gate oxide. Results shown in the fig 2. after a significant impact of rust stress. As a result of high gate voltage, transduction is rapidly reduced. The age of PBTI is calculated by the equation.

$$\text{Age(PBTI)} = \text{f}\left(\frac{1}{\text{V}_\text{s}}, \text{L}, \text{Temperature}, \text{Time}, \text{PBTI parameters}\right) \quad (2)$$

Whereas, V_s=Source Voltage and L= Channel Length of an individual MOS

(a) Stress: While in stress mode (Vgs = -Vdd), certain interface traps are emitted in the Si / dielectric interface. As a result, the transistor's initial voltage time proliferates [11].

(b) Recovery: At this stage, certain interface traps that are stemmed from the interface will be confiscated. Thus, the initial voltage will be condensed to its primary value (Vgs = 0). Note that the recovery mode is not absolutely substituted for the effect of stress mode, and therefore, the inclusive provoke of BTI is the positive change in the transistor's threshold voltage [9].

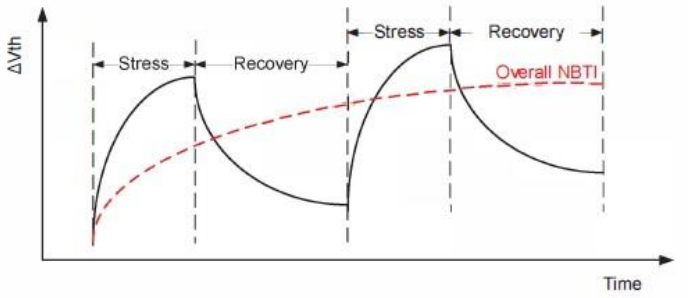

Figure 2: Stress and Recovery of MOSFET while electrons passing

3. Hot Carrier Injection (HCI)

HCI predominantly affects NMOS transistors after transmitting the NMOS gate-source. The carriers in the channel ensure subject to various electric fields while moving from source to drain [17]. Due to the high electric field in the drain, precision of the hot carrier can reach thermal limit above the drift speed (heat conductor). These hot carriers are subsided by the gate oxide interface; several electron holes are fabricated [12]. This produces slightly faster in the generated electrons and the $Si/Si0_2$ interface. This phenomenon increases the threshold voltage. The change of initial voltage prompted by the HCI can be evaluated as follows:

$$\Delta V_{th} = A_{HCI} \times \alpha \times f \times e^{\frac{V_{dd}-V_{th}}{t_{ox}E_i}} \times t^{0.5} \quad (3)$$

Where A_{HCI} is a technology constant, $\propto$ indicates the factor of activity and f is the frequency of operation. V_{th} and V_{dd} represent the initial voltage and supply voltage correspondingly. The thickness of the t_{ox} oxide, The E_i is similar to the affixed 0.8v/nm [15] and t is the overall operating time.

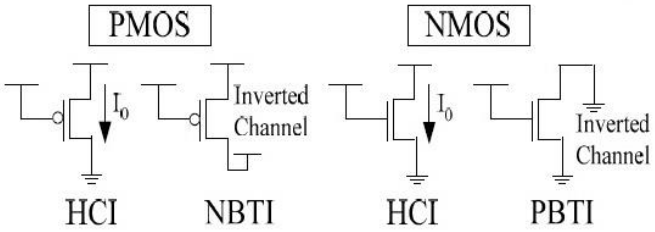

Figure 3: NBTI, PBTI & HCI effect on MOSFET's

4. Parameters Evaluated Methodologies

The censuring and pardoning of the capacitances at the oppress raises as the forceful power utilization to the transferring of bits from 'Low' to 'High' and 'High' to 'Low'.

Drain current

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_{TH})V_{DS} - \frac{{V_{DS}}^2}{2}\right) \quad (4)$$

Drain current at active region:

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_{TH})V_{DS}\right) \quad (5)$$

Drain current at saturation region:

$$I_D = \mu_n C_{ox} \frac{W}{L}\left(\frac{{V_{DS}}^2}{2}\right) \quad (6)$$

$$P_{DS} = fC{V}^2 \quad (7)$$

In circumstance of the dynamic power the frequency f, capacitance C and supply voltage V are the key factors.

The emanate of static current towards the ground from supply voltage without input degradation is leakage power. Three leakage mechanisms are sub threshold, band to band tunneling (BTBT) and gate oxide.

The static current flows from supply to ground level results in leakage power, the leakage ensues in various models like subthreshold, gate oxide and band to band tunneling [7].
Noise immunity is preserved in the proposed circuit, noise mostly pretends supply voltage which ensues into instabilities in the output response.

$$S_0(f) = 4kTR \qquad Where\ f \geq 0 \tag{8}$$

5. Literature Review

1. Yanwen Guo et.al [1] have analyzed the major impact of LUT in FPGA with the limitations of processing speed, density and configuration. In his research proposal, the memristor-based LUT to increase the performance of novel FPGA development.

2. Saman Kiamehr et.al [10] analyzed that transistor aging and reliability issues. In VLSI circuits in nano-meter technologies while the threshold voltage over time by transistor the delay and timing failures ultimately life span of the chip decreases. In his research, he investigates the effect of transistor due to PBTI and NBTI in various LUT by implementing the symmetric through SPICE simulations. In this author embedded two methods by Aging aware & timing analysis with combined NBTI and PBTI.

3. Subhadeep Mukhopadhyay et.al [15] analyzed the degradation of HKMG (High-κ Metal Gate) MOSFET under NBTI and PBTI stress in various conditions. Here, the author proposed an UF-MSM model to measure the delay characterised by threshold voltage (V_{th}). By experimentally explained the formation traps during BTI and stress applied to transistor in AC and DC voltage.

4. Santhosh Onkaraiah et.al [8] proposed a technology to improve the performance and reducing the power consumption by using CBRAM structure of LUT in FPGA. By good results, they decreased delay by 23% (approx) and power gained by 18% (approx).

5. Rahul et.al [14] designed and performed the reliability analysis of VLSI circuit in 45nm technology. Author evaluated the reliability models of NBTI, PBTI, HCI & TDDB.

6. Parthasarathy M.B. Rao et.al [12] here author performed the reliability analysis through input signal probability of LUT. Proposed two methods of BTI for aging of LUT. Finally, they preserved the lifespan up to an average 200% in FPGA mapped designs.

7. Seelam VSVPDK et.al [20] proposed a schematic diagram of comparator on 45nm technology and assigned the reliability techniques to find the degradation of an individual kind of mosfets by applying various threshold voltages.

8. Rahul et.al [13] performed the reliability analysis of a CMOS inverters circuits with the combination of RC model. Authors calculated the models of reliability in hot carrier injections, negative bias temperature instability and positive bias temperature instability with parameters of comparing delay, power and output voltage at only one particular nano scale.

9. S. Srinivasan et.al [18] aimed to increase the life span of FPGA chips for this reason they focused on two highly impacted hard errors i.e. time dependent dielectric breakdown and electro migration along with common reliability models of hot carrier effects and negative bias temperature instability. In addition to this authors shorted the solution of each failure of MOSFETS's to increase the working life.

10. E. Ahmed et.al [5] deigned a hybrid CBRAM based CMOS LUT to improve the stability of the FPGA that shows the significant changes from the normal CMOS structures and evaluated the comparison of reduces delay from compact structures and gain power by the demising the static power consumptions.

6. CLUT Proposed Technology

Here we proposed an FPGA based CLUT in various nanometer scales like 90nm, 45nm, 22nm and 11nm. We proposed this work to analyze the performance variation between the nanometer ranges. Hence, this schematic consists of 12 MOSFETs which are of 06 PMOS and 06 NMOS totally this schematic has 03 inputs and 01 output. However, the CLUT is more widely used in Spartan 3E [7]. It operated under the threshold voltage of 0.7v. It enhances the FPGA operation varies from different circuits like SRAM-LUT. C-LUT has an impact in the logic block of resources of sequential as well as combinational circuits [14]. In this proposed schematic the NMOS is slightly affected by PBTI under HCI aging and PMOS are highly affected by NBTI under HCI aging.

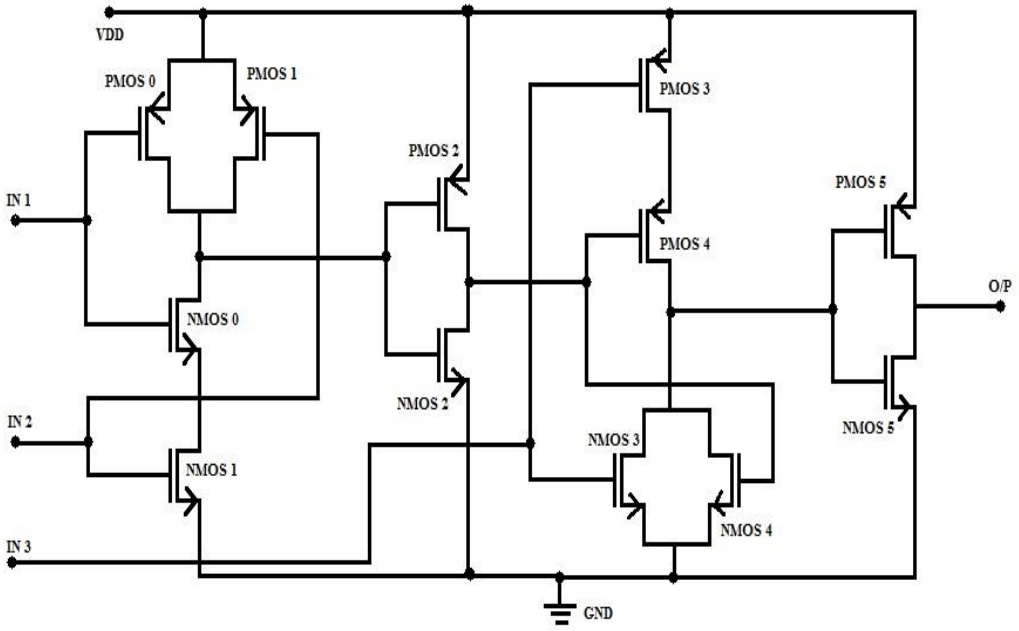

Figure 4: Proposed Design of 3-input CLUT circuit

The degradation of NBTI increases the principal value of the input threshold voltage of the PMOS device, which can lead to a drop in the flow of drain current, circulation and mobility [19]. It has been scrutinized that insertion of hydrogen in the gate dielectric is intensified mainly due to the effect of NBTI to degrade the penetration of boron from the poly gate P+ to the thin oxide and reduce the leakage at the gate. [5]. Principles are still a debate about the failure of the device. Let us consider any of the transistors for example PMOS0 undergoes NBTI degrades because its gate-source voltage is negative (-Vdd) and the source-drain voltage is zero volts are the condition for the degradation of NBTI [11]. The change in the initial voltage of PMOS0 directs to a dwindle in the performance of the CLUT cell, which affects several important performance parameters, such as SNM (Static Noise Margin) and leakage probabilities. The computation of voltage is essential in the internal nodes of the SNM to cut the contents of the cell.

7. CLUT Results in Various Nano Scale Range

To appraise the efficiency of proposed logic, we used different libraries which are compactable with cadence virtuoso simulator. It reduces the size of LUT's in FPGA of about 40% (depends upon the nano technology). We retrieved that there is a drastic change in their results as nano scale is reducing as shown below.

(a) Parameters accomplished

TABLE 1
PRESENTS THE LEAKAGE PARAMETERS OF 3-CLUT IN VARIOUS NANO METER RANGES

	Average Leakage Power (W)	Average Leakage Voltage (V)	Average Leakage Current (A)	Average Noise Margin (Av/sqrt(Hz))
90nm	8.82E-08	6.68E-01	4.18E-08	4.71E-16
45nm	4.48E-08	3.31E-01	2.14E-08	2.37E-16
22nm	2.20E-08	1.60E-01	1.10E-08	1.14E-16
11nm	1.09E-08	8.18E-02	5.30E-09	5.83E-17

Here, we calculated the parameters of 3-CLUT by decreasing the nano technology from 90nm-45nm-22nm-11nm. By these results, we observed an extreme in the average of leakage power, average leakage voltage, average leakage current and average noise margin by 50% individual scale which is illustrated in the above table 1.

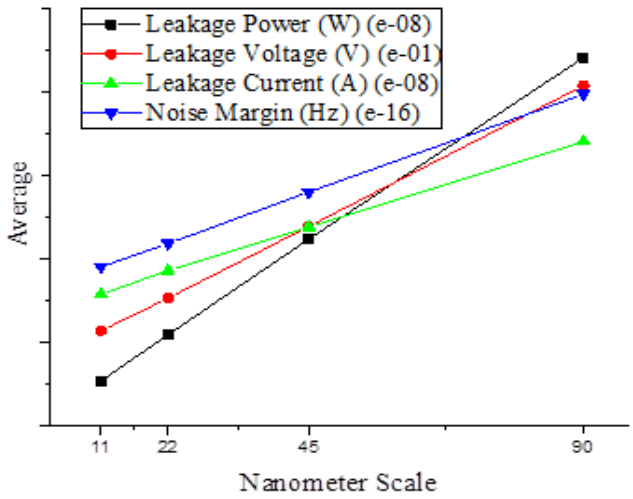

Figure 5: Graphical representation of Average leakage power, leakage voltage, leakage current and noise margin in reduction of Nano range

(b) NMOS under HCI aging

We studied NMOS under HCI aging in above section III in detail. By that analysis we executed the following results for a lifespan of 10 Years of individual NMOS's. Due to the formation of traps, it degraded by 50% of decreasing of nano scale. The results are evaluated in the below Table 2.

TABLE 2
NMOS UNDER HCI DEGRADATION IN REDUCTION OF NANO RANGE

	NMOS 0	**NMOS 1**	**NMOS 2**	**NMOS 3**	**NMOS 4**	**NMOS 5**
90nm	8.90E-74	4.18E-74	1.86E-63	1.47E-59	6.10E-59	1.76E-72
45nm	3.45E-74	2.72E-74	1.29E-63	7.36E-60	4.35E-59	9.80E-73
22nm	2.23E-74	1.05E-74	6.65E-64	3.68E-60	1.53E-59	4.10E-73
11nm	1.59E-74	7.43E-75	1.12E-64	1.84E-60	6.30E-60	1.30E-73

In the following graphical representation, it is clearly shown that every single NMOS has HCI effect. Due this effect the degradation of NMOS under HCI taken apart.

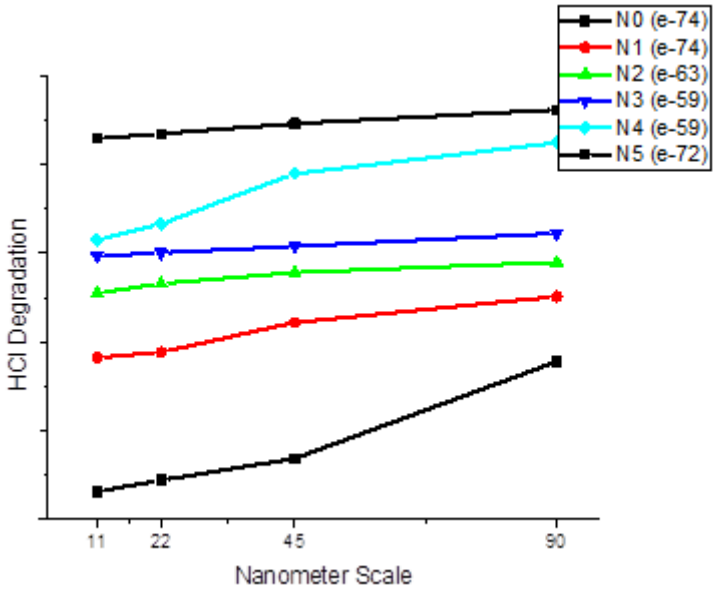

Figure 6: Graphical representation of individual NMOS under HCI in reduction of nano range

(c) PMOS under HCI aging

As we studied PMOS under HCI aging in section III in detail, by that analysis, we executed the following results for a lifespan of 10 Years of individual PMOS's. Due to formation of traps it degraded by 50% of decreasing of nano scale. The results are evaluated below Table 3.

TABLE 3
PMOS UNDER HCI DEGRADATION IN REDUCTION OF NANO RANGE

	PMOS 0	**PMOS 1**	**PMOS 2**	**PMOS 3**	**PMOS 4**	**PMOS 5**
90nm	6.98E-38	6.98E-38	1.00E-82	1.08E-78	0.00E+00	0.00E+00
45nm	4.49E-38	3.39E-38	0.00E+00	0.00E+00	0.00E+00	0.00E+00
22nm	2.11E-38	1.50E-38	0.00E+00	0.00E+00	0.00E+00	0.00E+00
11nm	8.73E-39	8.53E-39	0.00E+00	0.00E+00	0.00E+00	0.00E+00

In the following graphical representation, it is clearly shown that every single PMOS has HCI effect. Due this effect the degradation of PMOS under HCI taken apart.

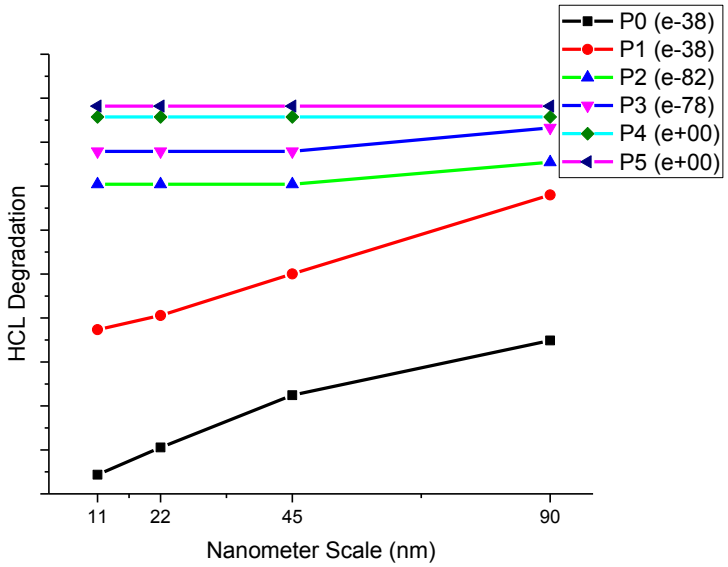

Figure 7: Graphical representation of individual PMOS under HCI in reduction of nano range

(d) NMOS under PBTI aging

In the academic tool, it shows that there is no effect on NMOS under PBTI aging. Due to no effect there is no degradation in NMOS. In detailed it was explained in section II.

(e) PMOS under NBTI aging

As we studied PMOS under NBTI aging in section II, it was explained in detail by that fundamental we executed the following results for a lifespan of 10 Years of individual PMOS's. Due to formation of traps it degraded by 50% of decreasing of nano scale. The results are evaluated below Table 4.

TABLE 4
PMOS UNDER NBTI DEGRADATION IN REDUCTION OF NANO RANGE

	PMOS 0	PMOS 1	PMOS 2	PMOS 3	PMOS 4	PMOS 5
90nm	4.12E-08	4.10E-08	8.48E-10	4.76E-10	8.06E-09	1.82E-09
45nm	2.36E-08	2.06E-08	5.24E-10	2.98E-10	4.83E-09	1.13E-09
22nm	1.03E-08	1.13E-08	2.12E-10	1.79E-10	2.92E-09	5.54E-10
11nm	7.15E-09	5.15E-09	1.76E-10	5.90E-11	1.01E-09	2.17E-10

In the following graphical representation, it is clearly shown that every single PMOS has NBTI effect. Due this effect the degradation of PMOS under NBTI taken apart.

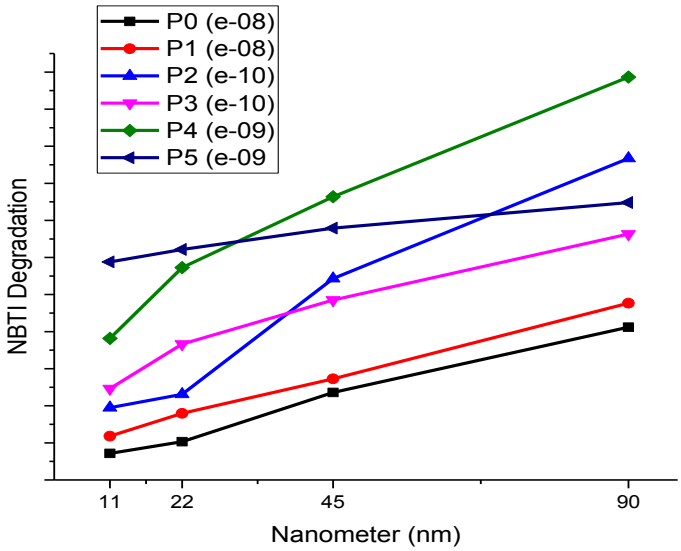

Figure 8: Graphical representation of individual PMOS under NBTI in reduction of nano range

8. Conclusion

The device endures to scale for superior integration with CMOS technology. However, decreasing feature sizes and chip designers are endeavoring to reduce the supply voltage to achieve the power targets in substantial multi-core methods, parameter variations become a serious problem. The variations of the parameters can be classified in general terms by device variation due to imperfections in the manufacturing process. A margin of large system is needed to maintain the stability of the circuit in interrogating of reliability. Designing the suffocate of reliability, in the long term requires the necessary design for future technical nodes and can reduce the excess of information when the performance and the robustness of the circuit increase. The aging of the transistor is an important peril of reliability for FPGAs fabrication in modern nanoscale VLSI technologies. In this paper, we analyzed the impact of transistor aging due to NBTI, PBTI and HCI in LUT moreover we analyse the parameters in various nano ranges by perceiving different accomplishments through detailed simulations of Cadence Virtuoso. The major conclusions of this consideration are encapsulated as the implemented LUT has designed in various nano scale range and analysis the aging effect by NBTI, PBTI, HCI and leakage performances. In this technique, we can identify the individual degradation of MOSFET's. The proposed technique can predict the life span of FPGA on average or more than 150 years.

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- ✓ Design, Automation and Test in Europe (DATE), Florence, Italy, March 25-29, 2019; web: https://www.date-conference.com/
- ✓ The 13th Annual International Conference on RFID (RFID), Phoenix, AZ, USA, April 2-4, 2019; web: http://2019.ieee-rfid.org
- ✓ The IEEE Custom Integrated Circuits Conference (CICC), Austin, TX, USA, April 14-17, 2019; web: http://ieee-cicc.org
- ✓ International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, May 26-29, 2019; web: https://www.iscas2019.org
- ✓ The 24th IEEE European Test Symposium (ETS), Baden-Baden, Germany, May 27-31, 2019; web: https://www.testgroup.polito.it/ets19/
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- ✓ Design Automation Conference (DAC), Las Vegas, NV, USA, June 2-6, 2019; web: https://dac.com/

Funding Opportunities		
Title	**Program Guidelines**	**Due Dates**
Understanding the Rules of Life: Building a Synthetic Cell **N** NSF-wide	18-599	Preliminary Proposal: December 28, 2018
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Enabling Quantum Leap: Quantum Idea Incubator for Transformational Advances in Quantum Systems (QII - TAQS) **N** NSF-wide	19-532	Letter of Intent: January 7, 2019
CISE Community Research Infrastructure (CCRI)	19-512	Letter of Intent: January 8, 2019
Integrative Strategies for Understanding Neural and Cognitive Systems (NCS) **C** Crosscutting	18-533	Letter of Intent: January 8, 2019
Cyberlearning for Work at the Human-Technology Frontier	17-598	Full Proposal: January 14, 2019
Formal Methods in the Field (FMitF)	18-596	Full Proposal: January 15, 2019
Expeditions in Computing	16-535	Full Proposal: January 16, 2019
Expeditions in Computing	18-528	Full Proposal: January 16, 2019
Partnerships for Innovation (PFI) **N** NSF-wide	19-506	Full Proposal: January 17, 2019
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Funding Opportunities		
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Harnessing the Data Revolution (HDR): Institutes for Data-Intensive Research in Science and Engineering - Ideas Labs (I-DIRSE-IL) **N** NSF-wide	19-543	Preliminary Proposal: January 28, 2019
Understanding the Rules of Life: Epigenetics **N** NSF-wide	18-600	Full Proposal: February 1, 2019
Designing Materials to Revolutionize and Engineer our Future (DMREF)	19-516	Full Proposal: February 4, 2019
Harnessing the Data Revolution (HDR): Data Science Corps (DSC) **N** NSF-wide	19-518	Full Proposal: February 4, 2019
National Science Foundation Research Traineeship (NRT) Program **N** NSF-wide	19-522	Full Proposal: February 6, 2019
Training-based Workforce Development for Advanced Cyberinfrastructure (CyberTraining) **C** Crosscutting	19-524	Full Proposal: February 6, 2019
Ideas Lab: Cross-cutting Initiative in CubeSat Innovations	19-530	Preliminary Proposal: February 8, 2019
Mid-scale Research Infrastructure-2 (Mid-scale RI-2) **N** NSF-wide	19-542	Letter of Intent: February 8, 2019

Funding Opportunities		
Title	**Program Guidelines**	**Due Dates**
EarthCube Office	19-523	Full Proposal: February 11, 2019
Computer Science for All (CSforAll:RPP)	18-537	Full Proposal: February 12, 2019
Spectrum Efficiency, Energy Efficiency, and Security (SpecEES): Enabling Spectrum for All **C** Crosscutting	19-529	Full Proposal: February 13, 2019
Navigating the New Arctic (NNA) **N** NSF-wide	19-511	Full Proposal: February 14, 2019
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National Robotics Initiative 2.0: Ubiquitous Collaborative Robots (NRI-2.0)	19-536	Full Proposal: February 19, 2019
Campus Cyberinfrastructure (CC*)	19-533	Full Proposal: February 20, 2019
CISE Community Research Infrastructure (CCRI)	19-512	Full Proposal: February 20, 2019
Enabling Quantum Leap: Quantum Idea Incubator for Transformational Advances in Quantum Systems (QII - TAQS) **N** NSF-wide	19-532	Preliminary Proposal: February 21, 2019
Cultivating Cultures for Ethical STEM (CCE STEM)	18-532	Full Proposal: February 22, 2019

Funding Opportunities		
Title	**Program Guidelines**	**Due Dates**
NSF Quantum Computing & Information Science Faculty Fellows (QCIS-FF)	19-507	Full Proposal: February 25, 2019
Integrative Strategies for Understanding Neural and Cognitive Systems (NCS) **C** Crosscutting	18-533	Supplement: February 26, 2019Full Proposal: February 26, 2019
Accelerating Research through International Network-to-Network Collaborations (AccelNet) **N** NSF-wide	19-501	Full Proposal: February 28, 2019
Advanced Computing Systems & Services: Adapting to the Rapid Evolution of Science and Engineering Research	19-534	Full Proposal: March 4, 2019
EarthCube:	16-514	Full Proposal: March 5, 2019
Future of Work at the Human-Technology Frontier: Core Research (FW-HTF) **N** NSF-wide	19-541	Full Proposal: March 6, 2019
Mid-scale Research Infrastructure-2 (Mid-scale RI-2) **N** NSF-wide	19-542	Preliminary Proposal: March 11, 2019
EPSCoR Research Infrastructure Improvement Track 4: EPSCoR Research Fellows (RII Track-4) **N** NSF-wide	18-526	Full Proposal: March 12, 2019
EarthCube:	16-514	Full Proposal: March 14, 2019
Historically Black Colleges and Universities Undergraduate Program (HBCU-UP)	18-522	Preliminary Proposal: March 19, 2019
Inclusion across the Nation of Communities of Learners of Underrepresented Discoverers in	18-529	Full Proposal: April 2, 2019

Funding Opportunities		
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Industry-University Cooperative Research Centers Program (IUCRC) **N** NSF-wide	17-516	Preliminary Proposal: April 17, 2019
Expeditions in Computing	18-528	Full Proposal: April 24, 2019
EMERGING FRONTIERS IN RESEARCH AND INNOVATION 2019	19-502	Full Proposal: April 25, 2019
Understanding the Rules of Life: Building a Synthetic Cell **N** NSF-wide	18-599	Full Proposal: May 13, 2019
Mid-scale Research Infrastructure-1 (Mid-scale RI-1) **N** NSF-wide	19-537	Full Proposal: May 20, 2019
Enabling Quantum Leap: Quantum Idea Incubator for Transformational Advances in Quantum Systems (QII - TAQS) **N** NSF-wide	19-532	Full Proposal: May 24, 2019
Research Experiences for Undergraduates (REU) **N** NSF-wide	13-542	Full Proposal: May 24, 2019
Ideas Lab: Cross-cutting Initiative in CubeSat Innovations	19-530	Full Proposal: May 30, 2019
Smart and Autonomous Systems (S&AS)	18-557	Full Proposal: June 3, 2019
Harnessing the Data Revolution (HDR): Institutes for Data-Intensive Research in Science and Engineering - Ideas Labs (I-DIRSE-IL) **N** NSF-wide	19-543	Full Proposal: June 19, 2019

Funding Opportunities		
Title	**Program Guidelines**	**Due Dates**
Industry-University Cooperative Research Centers Program (IUCRC) **N** NSF-wide	17-516	Full Proposal: June 19, 2019
NSF Quantum Computing & Information Science Faculty Fellows (QCIS-FF)	19-507	Preliminary Proposal: July 1, 2019
Partnerships for Innovation (PFI) **N** NSF-wide	19-506	Full Proposal: July 10, 2019
Faculty Early Career Development Program (CAREER) **N** NSF-wide	17-537	Full Proposal: July 17, 2019Full Proposal: July 18, 2019Full Proposal: July 19, 2019
Historically Black Colleges and Universities Undergraduate Program (HBCU-UP)	18-522	Letter of Intent: July 23, 2019
Mid-scale Research Infrastructure-2 (Mid-scale RI-2) **N** NSF-wide	19-542	Full Proposal: August 2, 2019
Computer and Information Science and Engineering (CISE) Research Initiation Initiative (CRII)	18-554	Full Proposal: August 14, 2019
Research Experiences for Undergraduates (REU) **N** NSF-wide	13-542	Full Proposal: August 28, 2019
Historically Black Colleges and Universities Undergraduate Program (HBCU-UP)	18-522	Letter of Intent: September 3, 2019
International Research Experiences for Students (IRES) **N** NSF-wide	18-505	Full Proposal: September 10, 2019
Computational and Data-Enabled Science and Engineering (CDS&E)		Full Proposal: September 16, 2019

Funding Opportunities		
Title	**Program Guidelines**	**Due Dates**
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Computer and Network Systems (CNS): Core Programs	18-569	Full Proposal: September 16, 2019
Computing and Communication Foundations (CCF): Core Programs	18-568	Full Proposal: September 16, 2019
Documenting Endangered Languages (DEL)	18-580	Full Proposal: September 16, 2019
Information and Intelligent Systems (IIS): Core Programs	18-570	Full Proposal: September 16, 2019
International Research Experiences for Students (IRES) **N** NSF-wide	18-505	Full Proposal: September 17, 2019
Research Experiences for Teachers (RET) in Engineering and Computer Science	17-575	Full Proposal: September 18, 2019
International Research Experiences for Students (IRES) **N** NSF-wide	18-505	Full Proposal: September 24, 2019
Computer and Network Systems (CNS): Core Programs	18-569	Full Proposal: September 25, 2019
Information and Intelligent Systems (IIS): Core Programs	18-570	Full Proposal: September 25, 2019
Innovations in Graduate Education (IGE) Program **N** NSF-wide	17-585	Full Proposal: September 27, 2019

Funding Opportunities		
Title	**Program Guidelines**	**Due Dates**
NSF Quantum Computing & Information Science Faculty Fellows (QCIS-FF)	19-507	Full Proposal: September 27, 2019
Computational and Data-Enabled Science and Engineering (CDS&E)		Full Proposal: September 30, 2019
Historically Black Colleges and Universities Undergraduate Program (HBCU-UP)	18-522	Full Proposal: October 1, 2019
Computational and Data-Enabled Science and Engineering (CDS&E)		Full Proposal: October 15, 2019
Industry-University Cooperative Research Centers Program (IUCRC) **N** NSF-wide	17-516	Preliminary Proposal: October 16, 2019
Graduate Research Fellowship Program (GRFP) **N** NSF-wide	18-573	Full Proposal: October 21, 2019 Full Proposal: October 22, 2019 Full Proposal: October 24, 2019 Full Proposal: October 25, 2019
Accelerating Research through International Network-to-Network Collaborations (AccelNet) **N** NSF-wide	19-501	Letter of Intent: October 30, 2019
Computational and Data-Enabled Science and Engineering (CDS&E)		Full Proposal: October 31, 2019 Full Proposal: November 1, 2019
CISE Community Research Infrastructure (CCRI)	19-512	Letter of Intent: November 12, 2019
Computer and Network Systems (CNS): Core Programs	18-569	Full Proposal: November 14, 2019

Funding Opportunities		
Title	**Program Guidelines**	**Due Dates**
Computing and Communication Foundations (CCF): Core Programs	18-568	Full Proposal: November 14, 2019
Information and Intelligent Systems (IIS): Core Programs	18-570	Full Proposal: November 14, 2019
Office of Advanced Cyberinfrastructure (OAC): Research Core Program	18-567	Full Proposal: November 14, 2019
Computational and Data-Enabled Science and Engineering (CDS&E)		Full Proposal: November 15, 2019
Historically Black Colleges and Universities Undergraduate Program (HBCU-UP)	18-522	Full Proposal: November 19, 2019
Collaborative Research in Computational Neuroscience (CRCNS)	18-591	Full Proposal: November 25, 2019
Historically Black Colleges and Universities Undergraduate Program (HBCU-UP)	18-522	Full Proposal: November 26, 2019
Computational and Data-Enabled Science and Engineering (CDS&E)		Full Proposal: December 5, 2019
National Science Foundation Research Traineeship (NRT) Program **N** NSF-wide	19-522	Letter of Intent: December 6, 2019
Smart and Connected Health (SCH)	18-541	Full Proposal: December 11, 2019
Industry-University Cooperative Research Centers Program (IUCRC) **N** NSF-wide	17-516	Full Proposal: December 18, 2019

Funding Opportunities		
Title	**Program Guidelines**	**Due Dates**
Cyberinfrastructure for Emerging Science and Engineering Research (CESER)		Full Proposal: Accepted Anytime
Experimental Program to Stimulate Competitive Research: Workshop Opportunities (EPS-WO) (EPS-WO) **N** NSF-wide	12-588	Full Proposal: Accepted Anytime
Facilitating Research at Primarily Undergraduate Institutions: **N** NSF-wide	14-579	Full Proposal: Accepted Anytime
Innovation Corps - National Innovation Network Teams Program (I-CorpsTM Teams) **N** NSF-wide	18-515	Full Proposal: Accepted Anytime
NSF/FDA SCHOLAR-IN-RESIDENCE AT FDA	18-556	Full Proposal: Accepted Anytime
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PolytechnicPositions	www.polytechnicpositions.com/

IP Core Protection and Hardware-Assisted Security for Consumer Electronics

IP Core Protection and Hardware-Assisted Security for Consumer Electronics presents established and novel solutions for security and protection problems related to IP cores (especially those based on DSP/multimedia applications) in consumer electronics. The topic is important to researchers in various areas of specialization, encompassing overlapping topics such as EDA-CAD, hardware design security, VLSI design, IP core protection, optimization using evolutionary computing, system-on-chip design and application specific processor/hardware accelerator design.

The book begins by introducing the concepts of security, privacy and IP protection in information systems. Later chapters focus specifically on hardware-assisted IP security in consumer electronics, with coverage including essential topics such as hardware Trojan security, robust watermarking, fingerprinting, structural and functional obfuscation, encryption, IoT security, forensic engineering based protection, JPEG obfuscation design, hardware assisted media protection, PUF and side-channel attack resistance.

About the Authors

Anirban Sengupta is an Associate Professor in the Discipline of Computer Science and Engineering at Indian Institute of Technology (IIT) Indore. He has authored more than 182 publications and patents. His is recipient of several awards/honors such as IEEE Distinguished Lecturer, Outstanding Editor Award, IEEE CESoc Best Research Award from CEM, Best Research paper Award in IEEE ICCE 2019, IEEE Computer Society TCVLSI Outstanding Editor Award in 2017 and IEEE TCVLSI Best Paper Award in IEEE iNIS 2017. He holds 12 Editorial positions in Journals. He is the Editor-in-Chief of IEEE VCAL (Computer Society TCVLSI), and General Chair of 37th IEEE Int'l Conference on Consumer Electronics (ICCE) 2019, Las Vegas.

Saraju P. Mohanty is a tenured full Professor at the University of North Texas (UNT) where he directs the "Smart Electronic Systems (SESL)". He has authored 280 research articles, 3 books, and invented 4 US patents. He has received various awards and honors, including IEEE-CS-TCVLSI Distinguished Leadership Award in 2018, IEEE Distinguished Lecturer by the Consumer Electronics Society (CESoc) in 2017, PROSE Award for best Textbook in Physical Sciences & Mathematics in 2016, and 2016-17 UNT Toulouse Scholars award. He is the Editor-in-Chief of the IEEE Consumer Electronics Magazine (CEM). He serves as the Chair of Technical Committee on VLSI, IEEE Computer Society. He has received 4 best paper awards and has delivered multiple keynote talks at various International Conferences.

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IP Core Protection and Hardware-Assisted Security for Consumer Electronics

The Institution of Engineering and Technology

IP Core Protection and Hardware-Assisted Security for Consumer Electronics

Anirban Sengupta and Saraju P. Mohanty

IEEE Consumer Electronics Magazine

Call for Articles for a Special Issue

Artificial Intelligence in Consumer Electronics

Guest Editors: Lia Morra, Fabrizio Lamberti, Anirban Sengupta, Saraju P. Mohanty

Artificial Intelligence (including Machine Learning and Deep Learning) is becoming ubiquitous components in Consumer Electronics. Virtual personal assistants, mobile devices, cameras, automotive electronics, wearable sensors and Internet of Things are among the many examples of technologies whose development is being powered by recent advances in Artificial Intelligence. At the same time, consumer devices are also enabler of AI development not only for the potential to collect large scale, real-life datasets, but also by providing innovative use cases and outlets where AI can be successfully applied. Nonetheless, the application of AI in Consumer Electronics brings at the forefront issues like robustness, user privacy protection, power consumption and dealing with noisy, uncurated data.

The goal of this Special Issue is to provide a platform for engineers, researchers, industrial experts and other stakeholders to appraise recent developments in the field and address related challenges. Contributions related to the practical, theoretical and engineering aspects of developing and deploying AI solutions are welcome on any applications of interest for the domain of Consumer Electronics (e.g. image enhancement, affective computing, processing of wearable sensor data, etc.). Articles pertaining ongoing technical developments, practical applications and use cases, user studies and evaluations, standardization efforts, current and future trend analysis, as well as next-generation technologies are welcome. Contributions tackling general issues spanning multiple applications are particularly welcome. Technical articles should be of general interest to an engineering audience and of broader scope than archival journal/transaction papers, as typically review and tutorial articles are suited to the Magazine.

Topics of interest for this Special Issue include, but are not limited to the following:

- AI and ML applications targeting consumer electronics
- Deep learning applications for mobile devices
- Learning from consumer-generated data
- Image and video processing
- AI for affective computing and human-centered interaction
- AI for Internet-of-Things and Smart Sensors
- Deep learning (hardware and software) for mobile and embedded devices
- AI and ML for Mixed Reality and HMI
- Virtual personal assistants
- Privacy-preserving artificial intelligence

- Safety and security of AI for consumer electronics

Submission Procedure:

Submissions should follow the IEEE standard template and should consist of the following: (i) A manuscript of maximum 6-page length (letter size paper with 11pt times font and 1 inch margin): A pdf of the complete manuscript layout with figures, tables placed within the text; (ii) A source file in Word or Latex format; (iii) High resolution original photos and graphics as JPEG files are required for the final submission. Images embedded in Word or Excel documents are not suitable; however, figures and graphics may be provided in a PowerPoint slide deck with one figure/graphic per slide. Articles which have been previously published at a conference need to have at least 40% new material, which need to be described in the cover letter accompanying the submission. The manuscripts need to be submitted online using the following URL: http://mc.manuscriptcentral.com/cemag.The authors need to select "*Special Section: Artificial Intelligence in Consumer Electronics"* in Step-1 of the submission process to ensure that the article is reviewed for this Special Call. For any questions, please contact guest editor Dr. Lia Morra, Email: lia.morra@polito.it

Schedule (tentative):

Submission Deadline: June 30, 2019

Author notification: Oct 30, 2019 (tentative)

Publication Date: Mid 2020 (tentative)

Guest editors:

Lia Morra (lia.morra@polito.it) Dipartimento di Automatica e Informatica, Politecnico di Torino, Italy

Fabrizio Lamberti (fabrizio.lamberti@polito.it), Dipartimento di Automatica e Informatica, Politecnico di Torino, Italy

Anirban Sengupta (asengupt@iiti.ac.in), Discipline of Computer Science and Engineering, Indian Institute of Technology (IIT) Indore, India

Saraju P. Mohanty (saraju.mohanty@unt.edu), Department of Computer Science and Engineering, University of North Texas

CONTACT: TCVLSI CHAIR | ASENGUPT@IITI.AC.IN 2018

Technical Committee on VLSI (TCVLSI), IEEE-CS

http://www.ieee-tcvlsi.org

What is TC-VLSI?

A technical committee of IEEE-CS serves as the focal point of the various technical activities within a technical discipline.

TCVLSI is a constituency of the IEEE-CS that oversees various technical activities related to VLSI.

Key People

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Anirban Sengupta, Indian Institute of Technology Indore
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TCVLSI Sister Conferences

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ARITH: www.arithsymposium.org
ASAP: http://www.asapconference.org/
ASYNC: http://asyncsymposium.org/
iSES: http://www.ieee-ises.org (formerly iNIS)
ISVLSI: http://www.isvlsi.org
IWLS: http://www.iwls.org
MSE: http://www.mseconference.org
SLIP: http://www.sliponline.org
ECMSM: http://ecmsm2017.mondragon.edu/en

Technically Co-Sponsored

ACSD: http://pn2017.unizar.es/
VLSID: http://vlsidesignconference.org

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Technical Scope Various aspects of VLSI design including design of system-level, logic-level, and circuit-level, and semiconductor processes

TCVLSI Offers
- Student travel grants
- Best paper awards
- Timely CFP info
- Free membership
- Venue to contribute to VLSI
- Circuits & Systems Letter
- News & View to VLSI Community

IET Journals
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Call for Papers

OPEN ACCESS PUBLISHING NOW AVAILABLE

SPECIAL ISSUE ON:

Hardware-Assisted Techniques for Security and Protection of Consumer Electronics

Editor-in-Chief: Andrew Tyrrell, University of York, UK

The EDA/hardware/VLSI community comprises people from diverse backgrounds (especially hardware and IP cores) leveraged for Consumer Electronics (CE). The electronics design industry is heading for a paradigm shift towards secured, reliable and low cost CE hardware as compared to conventional approaches. With this special section, we aim to present novel solutions for any security/protection problems related to hardware used in CE.

Consumer electronics comprising of high end devices ranging from digital cameras, multi-spectral cameras, smart tablets, and night vision cameras to smart meters, along with information and communication technology could make the emerging concepts of smart cities and Internet of Things (IoT) a reality. In the world of CE, security, privacy, and protection of hardware and its information are equally important. “Hardware-Assisted Security” is defined as the security/protection of hardware/intellectual property (IP) cores of CE devices or information by a hardware/system of CE devices. The term “security” encapsulates a broad theme that covers many aspects including hardware security, protection, privacy, trustworthiness, and IP protection and information security. System security may refer to the security of the system (e.g. a specific CE device) that handles the data or information.

Manuscripts should be scoped within the domain of Hardware-Assisted Security for CE devices and should be original manuscripts prepared in accordance to the normal requirements of *IET Computers & Digital Techniques*.

Topics covered include:

- Hardware security against Trojans for CE devices
- Forensic engineering based protection of CE hardware
- IP core/hardware security against NBTI attacks on DSP
- Hardware security/IP core protection against reverse engineering attacks for CE devices
- Protection mechanisms of IC/IP buyer
- Protection mechanisms of IC/IP seller
- Energy-efficient digital-rights management hardware for CE
- IP core protection of CE hardware
- Active and passive IP security of CE hardware
- PUF based security and protection methods of CE hardware
- Side channel attack resistant embedded systems, DRM systems

Submit your paper to the manuscript submission and peer review site via the following link:
www.ietdl.org/IET-CDT

Publication Schedule:

Submission Deadline:
28th February 2018
Publication Date:
November 2018

Guest Editors:

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University of Tennessee, USA
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ISVLSI 2018

Students Travel Support Awards

Alireza Mahzoon, University of Bremen, mahzoon@informatik.uni-bremen.de
Leslie Hwang, University of Illinois at Urbana-Champaign, lkhwang@illinois.edu
Xiaobang Liu, University of Cincinnati, liu2xg@mail.uc.edu
Zhiming Zhang, University of New Hampshire, zz1017@wildcats.unh.edu

IEEE COMPUTER SOCIETY ANNUAL SYMPOSIUM ON VLSI

Call for Papers

www.isvlsi.org

ISVLSI 2019

July 15-17, 2019
Miami, Florida



IEEE computer society

The IEEE Computer Society Technical Committee on VLSI

The IEEE Symposium on VLSI (ISVLSI) 2019 explores emerging trends, novel ideas and basic concepts covering a broad range of VLSI-related topics: from VLSI systems, tools and design methods at different abstraction levels, to bringing VLSI design and methods into new technologies such as nano and molecular devices and burgeoning application areas, such as hardware security, and artificial intelligence. Future design methodologies are also one of the key topics at the symposium, as well as new EDA tools to support them. Over three decades ISVLSI has been a unique forum promoting multidisciplinary research and new visionary approaches in the area of VLSI, bringing together leading scientists and researchers from academia and industry. The ISVLSI proceedings will be published by IEEE Computer Society Press. Selected papers from past editions have been subsequently published in special issues of top archival journals. ISVLSI has a good reputation of bringing together well-known international scientists as invited speaks. ISVLSI 2019 will continue the momentum and carry forward these well-established trends for further growth of the symposium.

Contributions are sought in, but not limited to, the following areas:

1) Circuits, Reliability, and Fault-Tolerance (CRT): Analog/mixed-signal circuits design and testing, RF and communication circuits, design for testability and reliability, adaptive circuits, interconnects, static and dynamic defect-and fault-recoverability, and variation-aware design.
2) Computer-Aided Design and Verification (CAD): Hardware/software co-design, logic and behavioral synthesis, simulation and formal verification, physical design, signal integrity, power and thermal analysis , statistical approaches.
3) Digital Circuits and FPGA based Designs (DCF): Digital circuits, chaos/neural/fuzzy-logic circuits, high-speed/low -power circuits, energy efficient circuits, near and sub-threshold circuits, memories, FPGA designs, FPGA based systems.
4) Emerging and Post-CMOS Technologies (EPT): Nanotechnology, molecular electronics, quantum devices, optical computing, spin-based computing, biologically-inspired computing, CNT, SET, RTD, QCA, reversible logic, and CAD tools for emerging technology devices and circuits.
5) System Design and Security (SDS): Structured and Custom Design methodologies, microprocessors/micro-architectures for performance and low power, embedded processors, analog/digital/mixed-signal systems, NoC, power and temperature aware designs, Hardware security, Cryptography, watermarking, and IP protection, TRNG and security oriented circuits, PUF circuits.
6) VLSI for Applied and Future Computing (AFC): Neuromorphic and brain-inspired computing, quantum computing, circuits and architectures for machine learning and artificial intelligence, methodologies for on-chip learning, deep learning acceleration techniques, applications for and use-cases of learning systems, sensor and sensor network, electronics for Internet of Things and smart medical devices.

ISVLSI program will include technical sessions by researchers and invited speakers, as well as a poster session. The keynotes, panels, special sessions and Student Research Forum are planned as well. Authors are invited to submit PDF files of full-length, original, unpublished manuscripts in IEEE proceedings format (no more than 6 pages) without author information through the on-line submission system: https://easychair.org/conferences/?conf=isvlsi2019.

Paper submission deadlines

Paper Submission Deadline: February 17,2019
Acceptance Notification: April 21, 2019
Submission of Final Version: May 12, 2019

Authors of selected top quality papers from ISVLSI 2019 will be invited to submit extended versions of these papers to a IEEE journal special issue. The selection process is based on reviewer feedback and quality of conference presentation.



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IEEE Transactions on Nanotechnology (TNANO) Special Section/Issue on the 18th IEEE International Conference on Nanotechnology (IEEE-NANO 2018)

Nanoscience and nanotechnology have rapidly established themselves as enabling disciplines within many disciplines including materials science, engineering, physics, chemistry, and biology. Following the success of the 18th IEEE International Conference on Nanotechnology (IEEE-NANO2018), IEEE Transactions on Nanotechnology (TNANO) is extending a Call For Papers for a Special Section /Issue reflecting the scope of the conference. Submitted manuscripts will undergo a full peer review process. Submissions are welcome but limited to NANO presentations. Authors who are attendees are requested to significantly expand the previous conference version to contain substantial new technical material, as per TNANO and IEEE restrictions on duplicated publications and the competitive acceptance process. Manuscripts for the TNANO Special Issue/Section must be submitted on-line using the IEEE TNANO manuscript template and "Information for Authors", via the IEEE Manuscript Central found at https://mc.manuscriptcentral.com/tnano. On submission to TNANO, authors should select the "Special Issue" manuscript type instead of "Regular Paper."

Submissions that reflect the Conference Scope and current state of the field are welcome in areas including:

- Micro-to- nano-scale bridging
- Nanobiology and Nanomedicine
- Nanoelectronics
- Nanomanufacturing and Nanofabrication
- Nano Robotics and Automation
- Nanomaterials
- Nano-optics, Nano-optoelectronics, and Nanophotonics
- Nanopackaging
- Nanoscale Metrology and Characterization
- Nanofluidics
- Nanomagnetics
- Nano/Molecular Heat Transfer & Energy Conversion
- Nano/Molecular Sensors, Actuators, and Systems
- Nanotechnology Safety, Education and Commercialization

Important Dates

- Submission of papers: **1 December, 2018**
- Notification of first review results: **1 March, 2019**
- Submission of revised papers: **15 April, 2019**
- Notification of final review results: **15 May, 2019**.

IEEE VLSI Circuits & Systems Letter

IEEE Computer Society Technical Committee on VLSI
(A Quarterly Publication of IEEE-CS TC on VLSI, TCVLSI)

Aim and Scope

The IEEE VLSI Circuits and Systems Letter (VCAL) is a quarterly publication which aims to provide timely updates on technologies, educations and opportunities related to VLSI circuits and systems. The letter is published four times a year and it contains the following sections:

Features: selective research papers within the technical scope of TCVLSI. Goal is to report novel interesting topics related to TCVLSI, as well as short review/survey papers on emerging topics in the areas of VLSI circuits and systems.

Opinions: Discussions and book reviews on recent VLSI/nanoelectronic/emerging circuits and systems for nano computing, and "Expert Talks" to include the interviews of eminent experts for their concerns and predictions on cutting-edge technologies.

Updates: Upcoming conferences/workshops of interest to TCVLSI members, call for papers of conferences and journals for TCVLSI members, funding opportunities and job openings in academia or industry relevant to TCVLSI members, and TCVLSI member news.

Outreach and Community: The "Outreach K20" section highlights integrating VLSI computing concepts with activities for K-4, 4-8, 9-12 and/or undergraduate students.

Have questions on submissions; contact EiC: Dr. Anirban Sengupta (asengupt@iiti.ac.in)

Join TCVLSI for FREE to be a part of a global community, visit: http://www.ieee-tcvlsi.org

More information at:
https://www.computer.org/web/tcvlsi/circuits-and-systems-letter
Submission details:
Please visit the website and use standard VCAL template to prepare the manuscript

IEEE computer society

The IEEE Computer Society Technical Committee on VLSI

Feature Member

Dr. Saraju P. Mohanty
Professor
Director, Smart Electronic Systems Laboratory (SESL)
Department of Computer Science and Engineering
University of North Texas

Saraju P. Mohanty is a Professor at the University of North Texas. Prof. Mohanty's research is in "Smart Electronic Systems" which has been funded by National Science Foundations (NSF), Semiconductor Research Corporation (SRC), US Air Force, Indo-USA Science and Technology Forum (IUSSTF), and Mission Innovation Global Alliance. He has authored 300 research articles, 4 books, and invented 4 US patents. His Google Scholar h-index is 29 and i10-index is 97. He has received 4 best paper awards and has delivered multiple keynote talks at various International Conferences. He received IEEE-CS-TCVLSI Distinguished Leadership Award in 2018 for services to the IEEE, and to the VLSI research community. He has been recognized as a IEEE Distinguished Lecturer by the Consumer Electronics Society (CESoc) since 2017. He was conferred the Glorious India Award in 2017 for his exemplary contributions to the discipline. He received Society for Technical Communication (STC) 2017 Award of Merit for his outstanding contributions to IEEE Consumer Electronics Magazine. He was the recipient of 2016 PROSE Award for best Textbook in Physical Sciences & Mathematics from the Association of American Publishers for his Mixed-Signal System Design book published by McGraw-Hill in 2015. He was conferred 2016-17 UNT Toulouse Scholars Award for sustained excellent scholarship and teaching achievements. He is the Editor-in-Chief (EiC) of the IEEE Consumer Electronics Magazine (CEM). He served as the Chair of Technical Committee on VLSI, IEEE Computer Society during 2014-2018, and was responsible to oversee a dozen of IEEE meetings including ASAP, ASYNC, ISVLSI, and iSES. More about his biography, research, education, and outreach activities can be obtained from his website: http://www.smohanty.org.

Q1. Tell us a little about your research area and what motivated you to get into it?

My current research is on Smart Electronic Systems. The research can be classified into the following inter-related thrusts: (1) Security and Energy Aware Internet-of-Things (IoT), (2) IoT-enabled Solutions for Smart Healthcare, and (3) Consumer Electronics for Smart Cities. The key aspects of the smart electronics are Energy-Smart, Security-Smart, and Response-Smart. Energy-Smart ensures that energy consumption of consumer electronics is minimal for longer battery life. Security-Smart deals with the security/protection of electronics systems as well as that of the information/media that these systems capture, process, or store. Response-Smart refers to accurate sensing, intelligent processing, and fast decision/actuation/response. Smart Electronics in the framework of IoT can provide 3Is (Instrumentation, Interconnection, and Intelligence) to the Smart Cities. Optimal combinations of hardware and software modules are explored for ESR-smartness and design/operation cost trade-offs of electronic systems. I have been engaged low-power hardware design for more than a decade. I have also worked on algorithms and hardware designs for security and copyright protection for a long time. My current research motivation is to work more close to applications domain and have stronger and fast impact on society. Thus, smart healthcare, smart cities application domains are of interests to me.

Q2. What are some of your proudest accomplishments?

There are many things that come to mind. In 1997, joining Indian Institute of Science (IISc) Bangalore that admits only top less than 1% students from India was one proud moment. In fact, during MS research, the articles that I had published later helped me to get USA Permanent Residency in EB1 category in a matter of a month since when I applied in 2004. It was a very good feeling when I built the proof of concept of Secure Digital Camera (SDC) in 2004. SDC with integrated security and protection capabilities and energy-efficient design is a demonstration of energy and security trade-offs which is essential for the current edge computing which is post-cloud-based-IoT computing paradigm. The architecture-level approaches for power transience/fluctuation minimization during deign exploration that I did around 2003 to 2005 has made me feel good. It was one of its kind during high-level synthesis to capture power, power-fluctuation, process variation unified fashion at early design flow. Moreover, reducing power fluctuation to make uniform power profile can essentially be a tool for power trace obfuscation to reduce the side channel attack through power analysis to make security aware DSP design. Another work that I am proud is iVAMS (Intelligent-Metamodel Integrated Verilog-AMS) which can be used for ultra-fast and yet accurate simulation, design exploration, optimization, and verification of analog/mixed-signal components. The key idea was to build intelligent metamodels (which is essentially machine learning models) from the silicon data of the integrated circuit and integrate them in Verilog-AMS to make simulations of large designs feasible with silicon accuracy. Thus, the use of machine learning models (ML) for silicon bigdata was done in this work way before current data-science community talked about bigdata with of course a variety of datasets. I was proud when USCIS approved my self-petition in 2005 for USA permanent residency in EB1 outstanding researcher category in 3 weeks time. Receiving the 2016 PROSE Award for best Textbook in Physical Sciences & Mathematics category from the Association of American Publishers (AAP) for his book titled "Nanoelectronic Mixed-Signal System Design" published by McGraw-Hill in 2015 was a proud moment. To be listed 42 distinguished Non-resident Indians (NRI) and Indian origin who have excelled in their careers to receive the Glorious India Awards in 2017 was a proud moment. It was done during May 2017, the Glorious India Expo took place at the New Jersey Convention & Exposition Center, Edison, USA by carious India and USA based organizations including Innovative Council of Indian Tourism, Make in India, Incredible India, and US-India Business Council were sponsoring entities. I am proud to Chair of IEEE-CS TCVLSI as well as to serve that the Editor-in-Chief (EiC) Consumer Electronics magazine to serve our research community.

Q3. How do you see your research field shaping up and what are the major directions?

I am currently interested in smart electronics research in the smart cities applications domain. Automated monitoring of various city parameters for decision making. In smart healthcare, automatically monitoring food intake to determine calories and automatically suggest future diet for healthy living is one area that I have been researching. In smart healthcare, monitoring physiological activities for stress level detection and management. Another interesting work is early detection (or even prediction) of seizure and then onsite drug delivery in a IoT framework. I consider security, privacy, energy-efficiency, response-time, intelligence, design-cost, and operational-cost are important for but mutually conflicting requirements in smart electronics. For example, a security solution in an implantable electronics can cause energy issues. A security mechanism for a smart car or an UAV can have impact on their battery life (energy), payload, range, and response time. Research in anyone of these objectives and/or their combined forms are directions. Specifically, system design flow accounting one and more of these requirements as objective and/or constraints is an important research direction. Hardware-assisted security in which hardware protects itself, protects the system, and also protects the information being processed by the system is an

important research direction. Appropriate PUF design, PUF based security protocols, and integration of PUF in the IoT platform is important research. Blockchain technology integration in electronics for security and other applications is an involving trend. Blockchain inherently need not be an efficient solution. It can be effective when completely untrusted entities are working together. However, the blockchain technology is extreme energy hungry. For example, mining of 1 bitcoin (that uses blockchain with proof-of-work as the consensus algorithm) needs energy equivalent to 2 years' consumption of a typical US household. The proof-of-work (PoW) even in high-performance servers can take significant time to run. Blockchain technology that can run using a very minimal resource and energy is a research direction. Edge computing instead of classic cloud-based IoT computing for energy efficient and fast response is a research direction.

Q4. What advice would you give to junior researchers and graduate students?

The best advice that I can think of for researchers is that time is crucial and spend is wisely. For the graduate students, I advise to work hard and be productive as soon as possible. It is crucial to discuss research with your mentor and complete your degrees on time. It is good to spend time on hard and challenging problems than easy and incremental problems. Understanding the research problem is critical before trying to solve it. If you understand the problem, then your research is half done. For junior researchers (faculty), I advise to maintain balance between professional and personal aspects is important. I think maintaining a balance between different aspects of research such as funding, publishing, and student graduation is key for long-term sustainability. Similarly, teaching both undergraduate and graduate classes is important for a faculty as it is a medium for research dissemination. Professional services are helpful for networking as well as for leadership skills.

Q5. What profession would you be in if you weren't in this field?

I always wanted to be in academia. Right from the first day of my undergraduate studies I planned to be a faculty in an Engineering Institute. The other option that I was thinking is a research scientist in a National lab. However, it reminds me that my father always wanted me to join Indian Administrative Services (IAS). It is through a National level selection process and appointment is done by the President of India. The position seemed to have lots of power. However, I always used to tell him that I will be an Engineering Professor: I like Engineering and to train others on the same.

Q6. Any final thoughts?

There is no substitute to working hard and smart.

IEEE Computer Society Technical Committee on VLSI (TCVLSI)

Member News

- ✓ **Dr. Anirban Sengupta** awarded **IEEE Computer Society Distinguished Visitor** in Jan 2019.

- ✓ **Dr. Anirban Sengupta and Dr. Saraju Mohanty** co-authored book on **“"IP Core Protection and Hardware-Assisted Security for Consumer Electronics”** published by **IET (UK)** in Jan 2019.

- ✓ **Dr. Anirban Sengupta** and **Dr. Saraju Mohanty** invited as panelists on “Cybersecurity” in **37th IEEE International Conference on Consumer Electronics (ICCE) 2019**, Las Vegas USA.

- ✓ **Dr. Himanshu Thapliyal** organized a panel on “Cybersecurity” in **37th IEEE International Conference on Consumer Electronics (ICCE) 2019**, Las Vegas USA.

- ✓ Dr. Saraju Mohanty delivered a **keynote** on “Smart City” in **37th IEEE International Conference on Consumer Electronics (ICCE) 2019**, Las Vegas USA.

- ✓ **Dr. Anirban Sengupta** from Indian Institute of Technology (IIT) Indore invited to serve on the Editorial Board of **IEEE Transactions on VLSI Systems** as Associate Editor from Jan 2019.

- ✓ **Dr. Anirban Sengupta** from Indian Institute of Technology (IIT) Indore joined Editorial Board of **IEEE Transactions on Consumer Electronics (TCE)** as Associate Editor from Jan 2019.